Silicon-On-Insulator

A perspective on low-power, low-voltage supervisory circuits implemented with SOI technology.

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The magic term of SOI is attracting a lot of attention in the design of high-performance circuits. SOI offers speed, reliability and hardness beyond traditional technologies.

SOI's performance parameters can be attributed largely to overall capacitance reduction as well as lower SOI device leakage. This creates the ideal opportunity for implementing SOI in sophisticated IC designs operating under LP-LV conditions. The focus of this article is to present an overview of SOI technology applied to design of a special class of ultra LP-LV devices — supervisory circuits. Such circuits are emerging as prime candidates for development using advanced SOI technology processes.

Basic Principles and Features of SOI

The first part of this article is devoted to the basic features of SOI technology. A comparative conventional CMOS process (also labeled as "bulk" process) will be introduced while describing the semiconductor structures.

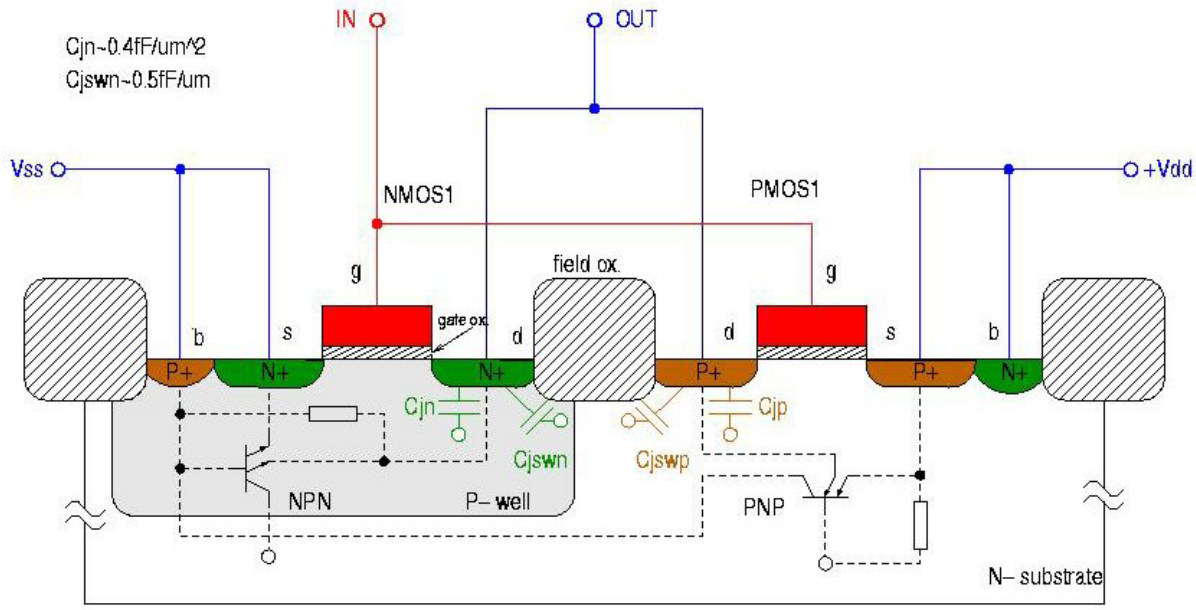

Figure 1.Cross-section of a "bulk" CMOS inverter (including parasitic bipolar scheme for latchup).

First, consider the most common structure of a CMOS inverter fabricated in conventional bulk technology (see Figure 1). The structure is placed on a standard silicon wafer that also functions as the electrical substrate. Obviously, it creates the fourth electrode (bulk-b) of the PMOS1 transistor directly. The bulk electrode is then connected to PMOS1 source (s), which is on $+V_{dd}$ potential. The second transistor, NMOS1, is situated in a separate well P-type to electrically isolate its bulk electrode from the whole N-substrate. The bulk of NMOS1 is connected to V_{ss}, together with the source electrode (s). The equivalent electrical scheme of the whole inverter is depicted in Figure 2a. In fact, the electrical isolation between the opposite-type MOS transistors is made by a substrate diode as well as field oxide (see Figure 1).

However, the existence of a PN junction in the bulk CMOS structure implies non-ideal behavior. First, the barrier capacitance of the reverse-polarized junction (for instance the substrate diode in a MOS transistor) is relatively high and may significantly decrease the circuit speed. Second, leakage

current of the junction may not be negligible in some cases, especially when the circuits operate in the low-power, low-voltage region. The last important disadvantage of the bulk CMOS structure is the possible device latchup[1].

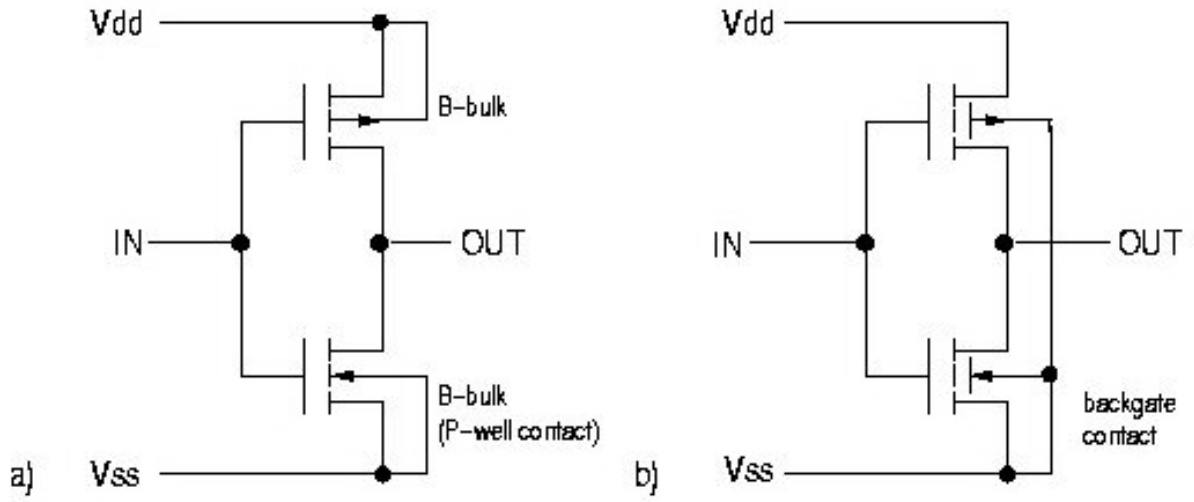

Figure 2. Electrical scheme of bulk (a) and SOI (b) CMOS inverter.

Figure 1 already encloses the parasitic bipolar scheme valid for a CMOS bulk structure. Note that since the MOS structure is symmetrical, each bipolar device has two emitters. It can be seen that the bipolar scheme creates a simple thyristor model. The fictive thyristor is connected directly between $+V_{dd}$ and V_{ss} potential and can be turned on by a random negative pulse applied to the OUT terminal. This turns on the vertical NPN transistor, transferring the positive feedback mechanism to the lateral PNP device. In this way, the current through V_{dd} is steadily increasing, even though the random pulse on the OUT terminal might no longer be present.

Consequently, the circuit has the potential to be damaged by a very high value of the supply current. To prevent the latchup, several sophisticated (but also high-cost) processes, such as deep trenches or double well, were developed. However, in spite of these developments, SOI technology can offer a much better system solution, improving the process and device features.

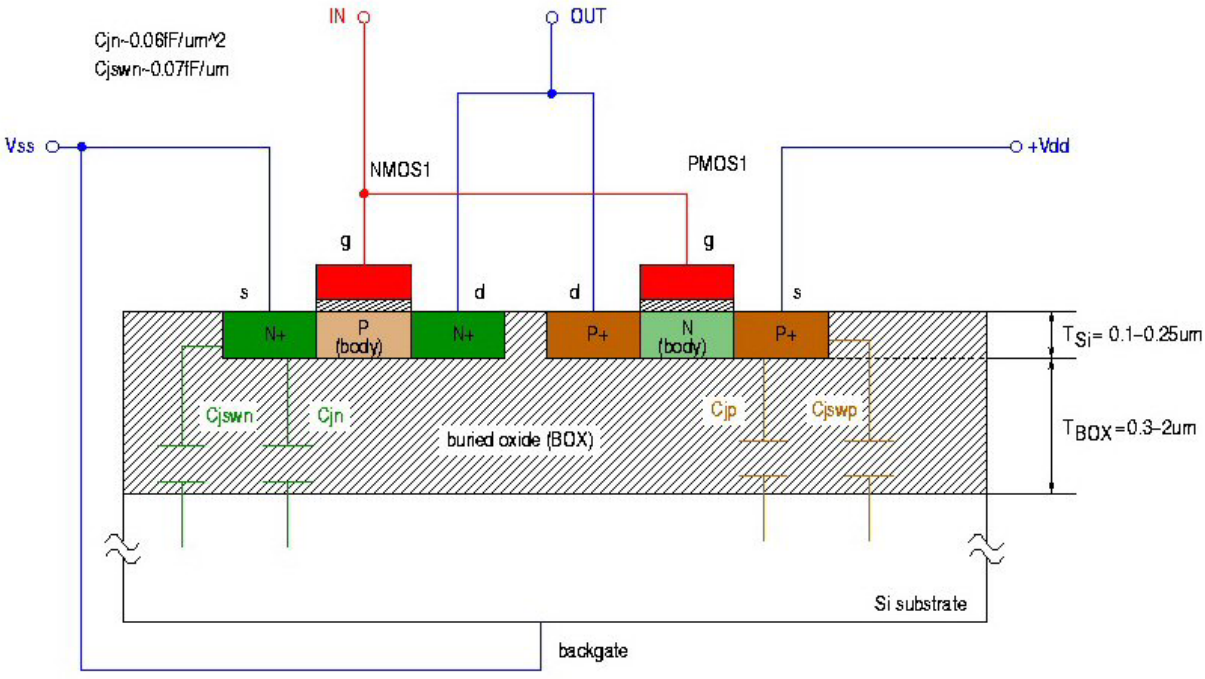

Figure 3. Cross-section of a thin-film SOI CMOS inverter.

A cross-sectional view of the SOI CMOS inverter is shown in Figure 3. Note that both views of Figure 1 and Figure 3 are basically schematic in nature (some technology masks were omitted to make the pictures more intuitive).

Fundamentally a standard silicon wafer can be used in SOI process. The main functional difference is that with SOI. The original silicon wafer only provides the mechanical function that creates the underlying (carrying) pad. To create the complete SOI wafer, an insulation layer (buried oxide — BOX) and a very thin silicon film must be deposited on the silicon. For SOI wafer fabrication, many advanced methods (such as SIMOX and UNIBOND[2]) are presently used. With SOI, all the functional structures are created within the thin single-crystalline layer (T_{Si}), placed above the insulator. As shown in Figure 3, each MOS device is now placed in a separate silicon film island, naturally isolated by surrounding BOX. Therefore no diffused well nor is a field oxide deposition needed to electrically isolate the devices. In practice, the isolation is performed mainly by LOCOS or shallow trenches[3]. The silicon substrate is separated from the silicon film by relatively thick buried oxide (the electrical contact on silicon substrate is called the back gate, and is usually common for the whole chip. This is the main difference from classical bulk process where every well might have separate contact. (Potentially, the diffusion wells can be also shared on the condition that they follow some specific circuit and technology rules).

This difference is also obvious from the inverter circuit scheme shown in Figure 2b. However, the SOI structure enables efficient cancellation of some undesired parasitic effects. The device latchup is cancelled because all the functional structures (in this case, MOS transistors) are separated from the semiconductor substrate: the coupling between the back gate and the body of a transistor remains capacitive only, with no substrate junction. And, as will be discussed later, the substrate and device capacitances are significantly reduced and the device leakage decreases because of the lack of well and substrate diodes. This is not the only innovation using SOI. In Figure 4a, the so-called GAA MOSFET is depicted, which can achieve up to five times better transconductance than conventional planar structures[4].

This is possible due to efficient gate control of the carrier volume flowing through the channel. In Figure 4b, the stacked structure of MOS devices is depicted illustrating the fact that the SOI wafer structure can be periodically repeated in the vertical direction, as well. This creates an alternative way to significantly shrink the device structures (could it be used within the next ten years after necessary process improvement[5]?)

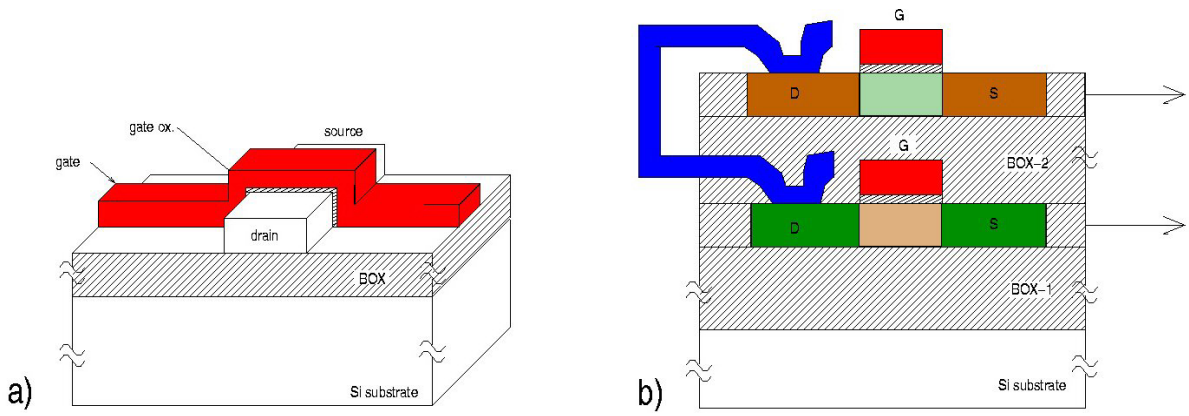

Figure 4. Innovative 3D SOI devices: a) GAA MOSFET, b) stacked-transistor structure.

SOI Technology Compared to Bulk

Before discussing SOI devices and structures in LP-LV circuits, it is prudent to summarize some general advantages and benefits of SOI implementation. Some SOI drawbacks and the way they could be compensated or avoided will also be presented.

The prospective advantages of SOI can be presented in the following discussion.

Higher speed of SOI is a consequence of effective elimination of vertical as well as sidewall parasitic capacitances. In a general MOS structure, the dominant parasitics are gate and source

(drain) capacitance. These can be further divided into several components. With SOI, gate capacitance behavior is similar to the bulk case (although some differences are observable due to floating body and back gate effects[3]). With SOI, a more reasonable case occurs in drain and source capacitances, when compared to bulk structures (compare Figure 1 to Figure 3). With SOI, the sidewall ($C^{jswn,p}$) as well as vertical ($C^{jn,p}$) capacitances are dramatically reduced by the existence of thick BOX between the silicon film and silicon substrate. The drain and source capacitance value can be reduced by up to a factor of seven, compared to bulk. Therefore, extremely low propagation delays can be achieved when implementing SOI in digital circuits (recently, less than 8 ps inverter delay was obtained[6]).

• Higher integration density. The possibility of effectively shrinking SOI devices stems from the fact that no well and required substrate taps and latchup protection rings are needed. Also the area of the field oxide used for lateral inter-device insulation is reduced significantly.

The use of shallow trenches or the LOCOS process seems to be more compact compared to complicated isolation techniques such as deep trenches often used in bulk[1,3].

• Higher reliability and hardness. The higher reliability of SOI devices is mainly due to the fact that latchup effects are eliminated. Referring to hardness, it has been proven that SOI MOSFETs are extremely robust to radiation effects and other physical exposure[2]. This is supported by the fact that in exposed circuitry, most of the electron-hole pairs are generated in thick silicon. Also the BOX layer underlying the structures can create a natural shield against the exposure.

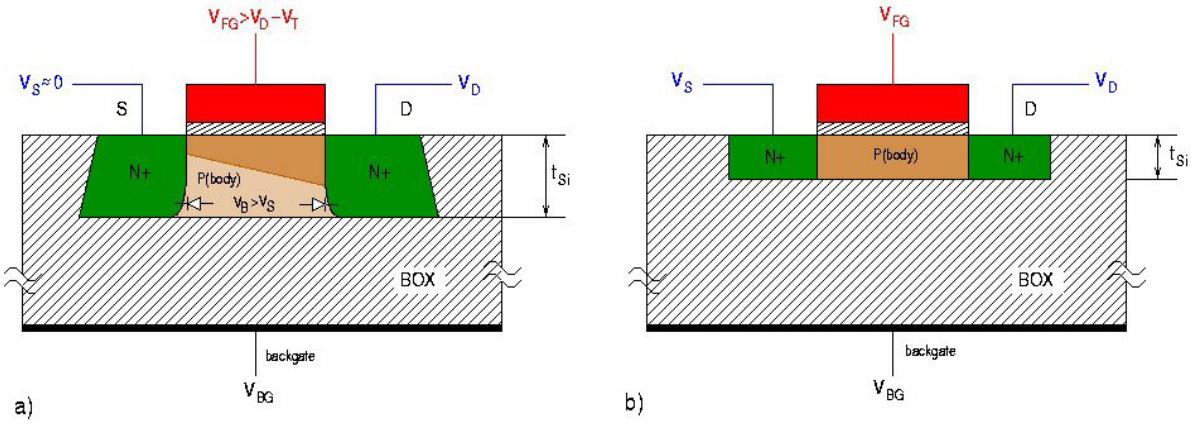

Figure 5. a) Partially depleted (thick film) SOI MOSFET with kink effect; b) fully depleted (thin film) device.

A Downside

However, there are some disadvantages to SOI technology when discussing advanced circuit or technology rules.

There are two basic classes of SOI devices. These are PD and FD devices (Figure 5 shows both technology variants on SOI MOSFET). The criterion for each device class is the silicon film thickness, compared to the maximum depth of a charge depletion region, extends to a transistor body. In Figure 5, the depletion charge under the device gate (also called the front gate) is noted with gray. Note that there is also a second gate interface created by the common back gate. In partially depleted SOI MOSFETs, the depletion charge does not extend to the back gate interface and a neutral region subsists in the device body. This in fact occurs in a generalized SOI MOS structure with silicon film, t_{Si}, thicker than twice the maximum depletion depth x_{dmax}[3]. Therefore PD devices are often labeled as thick-film.

In contrast, the fully depleted SOI MOSFETs (see Figure 5b) are characterized by a full charge depletion covering the whole transistor body. These devices are often called thin-film, since in generalized structure, the condition $t_{Si}<x_{dmax}$ is fulfilled. Note that the SOI CMOS inverter depicted in Figure 3 belongs to the thin-film device family. The first parasitic effect is related only to the partially depleted SOI devices.

Speaking Kink

Kink effect belongs to the so-called floating body effects. Except for some special cases[3], there is no equivalent effect in bulk because of connected transistor body either to the substrate or a well.

Consider the thick film PD SOI MOSFET depicted in Figure 5a. From the impact ionization caused by high electric field near the drain region, a part of the majority carriers (holes) can migrate to the transistor body. This is due to the potential of V_B being, originally, very close to V_S, which corresponds to zero.

Nevertheless the whole migration results in a local increase of the body potential V_B. In the case where the voltage drop across the body-source diode is high enough, the junction may be turned on, giving rise to a decrease of the transistor threshold voltage. However, it results in a current drop called "kink" in the drain device characteristics (see Figure 6). The mechanism described above is the so-called "first kink" in a SOI device[7]. This can be a serious disadvantage in precision analog design as well as in low power digital design.

In practice, there are several ways to avoid the kink effect in PD SOI. The most common one is to create the so-called body contact. Fortunately, it can be shown that FD SOI devices do not suffer from the kink effect, which is a primary advantage of the fully depleted SOI processes.

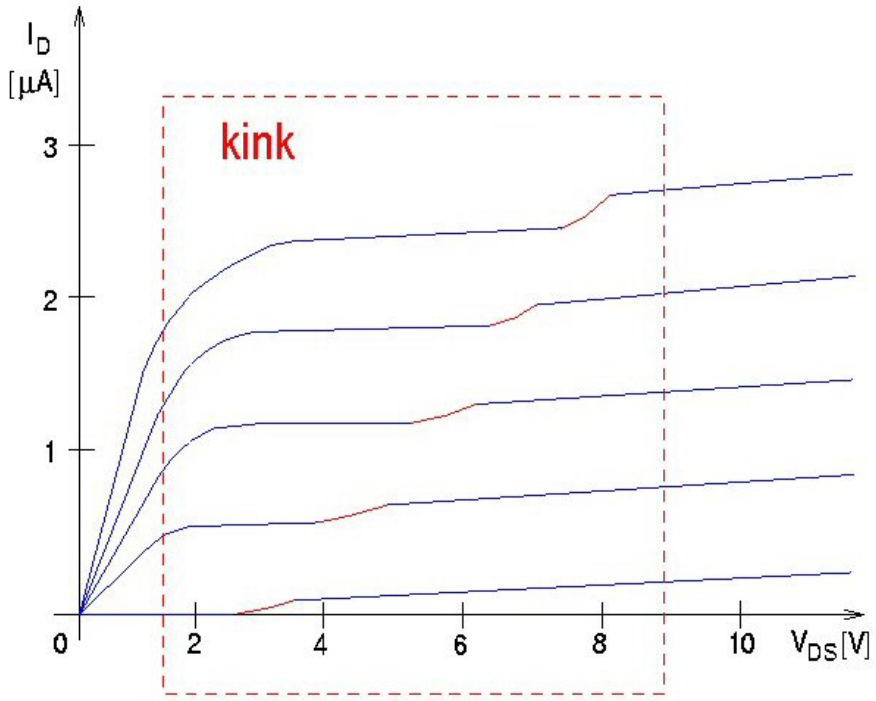

Figure 6. First kink in PD SOI MOSFET.

Heat Issues

Self-heating is the effect generally present in SOI due to the poor thermal properties of SOI substrates. Notice that SOI transistors are thermally insulated from the substrate by the buried insulator (BOX). Consequently, removal of the Joule heat generated within the devices is less efficient than with bulk. As a result, a negative resistance region can be observed in drain device characteristics while applying large V_{GS} and V_{DS} voltage values. This is a result of mobility and drain current decrease caused by intensive internal heating within the device. Note that the impact of the self-heating also depends on the scanning speed while measuring the device characteristics.

Some experiments report that self-heating does not occur in pulse mode or applying slew rate higher than 20 V/µs. This is due to the fact that the time during which the power is dissipated is much shorter than the thermal time constant of the devices. Therefore the impact on high speed devices and circuits is not that decisive.

Hysteresis and Latch Effects

Hysteresis and latch effects in SOI MOSFET are observable while operating at the border between the weak and strong inversion region. It can be shown[7] that for large V_{DS} voltage values observable hysteresis in gate characteristics occur. Moreover, in some rare cases, hysteresis is also supported by the memory effect. It means that the transistor does not turn off when the gate voltage goes to zero. This effect is related to the parasitic bipolar structure in SOI and can be avoided with some advanced technology procedures[7].

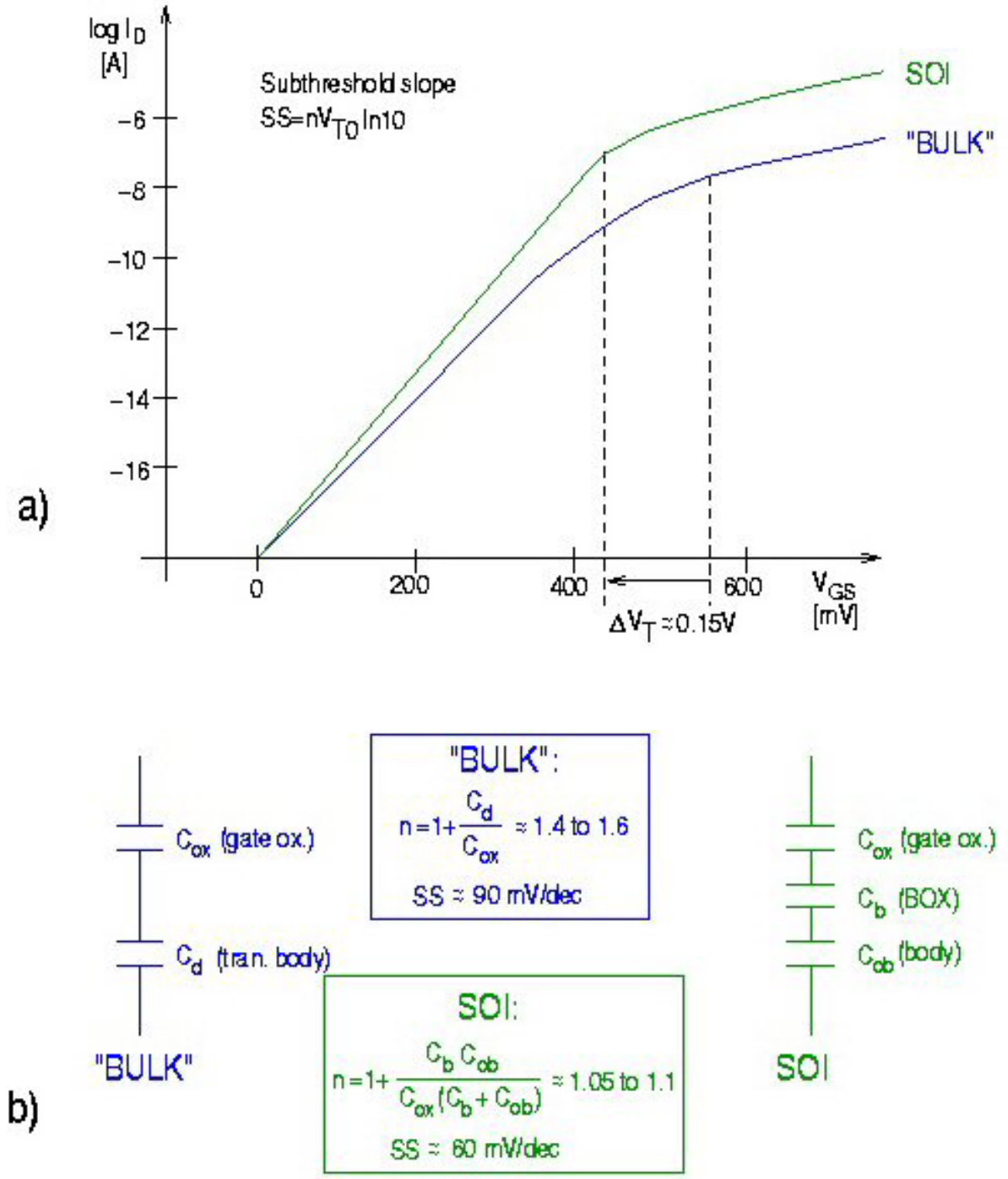

Figure 7. Comparison of SS and VT for "bulk" and SOI: a) sub-threshold gate characteristics; b) corresponding equations.

SOI Advantages for Use in Low-power, Low-voltage Systems

This section discusses the benefits of SOI when operating in the LP-LV region of the device. From this perspective the SOI device features will be evaluated. Some specific features will be introduced that derive from the technological structure.

In LP-LV circuits, the device operation point is set near the sub-threshold region (more exactly, to the weak inversion or the border between strong and weak inversion, respectively). In a MOS transistor, the gate-to-source voltage is set near device threshold V_T and the drain voltage is reduced, in comparison with the device breakdown value. The current values are lowered as well to obtain the minimum device power. At this point, the values in the range of nA are normal and can be comparable to the leakage in technology structures. To fulfill the LP-LV conditions, it is of the utmost importance to improve the device and technology features to obtain the desired performance. Following is the discussed of how LP-LV requirements are addressed on advanced SOI processes.

Fundamental LP-LV Advantages

Operating in LP-LV mode addresses many of the SOI drawbacks described in the previous section. Due to the restricted range of the drain voltage and operation near the device threshold, the kink effect as well as self-heating will disappear from the device characteristics. Even so, it is preferred to use either the advanced FD SOI processes or optimized PD SOI using body contact to negate the undesired kink mechanism.

The device latch or memory effect usually appears at high drain voltage. Therefore will be virtually cancelled in LP-LV devices.

The lower sub-threshold slope of SOI is a result of a reasonable capacitance arrangement. In a weak inversion, the sub-threshold slope is defined as the change of the gate voltage, V_{GS}, needed for the one-decade increase of the drain current I_D (a comparison for bulk and SOI is shown in Figure 7). The coefficient n is derived from the static capacitances in the structure and its value is lower in the case of SOI (mainly due to the low serial capacitance created by the buried oxide layer). However, a lower value of n implies a lower sub-threshold slope in the case of SOI vs. bulk.

This has several advantages. First, it means better gate control of the drain current in the sub-threshold operating region can be achieved. Second, it leads to a potentially lower device threshold voltage, V_T, of the SOI MOSFET, when compared to its bulk counterparts.

Lower threshold voltage can be explained via the drain device characteristics near the point of the strong inversion. From Figure 7 it can be seen that a lower sub-threshold slope corresponds to a lower threshold value of the SOI MOSFET. Obviously, a lower V_T value is reasonable for LP-LV circuit applications. It enables the circuit to operate at a lower V_{dd} and lead to an increase of drain saturation current (for a given gate voltage). At this point, significant reduction of the gate voltage, to operate under low drain currents, leads to further reduction of power dissipation.

In short-channel MOSFET devices, the influence of the real shape of the drain-source conducting channel becomes significant. In such a short-channel device, loosening the gate control of only a small fraction of the channel can cause a large roll-off of the device threshold voltage. However, in SOI, short-channel effects are effectively suppressed due to geometrical and structural reasons[3].

Lower SOI device leakage can be seen as a consequence of a more straightforward implementation of device isolation techniques than with bulk. As was previously discussed in the section concerning SOI versus bulk comparison, lower leakage is also supported by the fact that no well and substrate junctions are present in SOI.

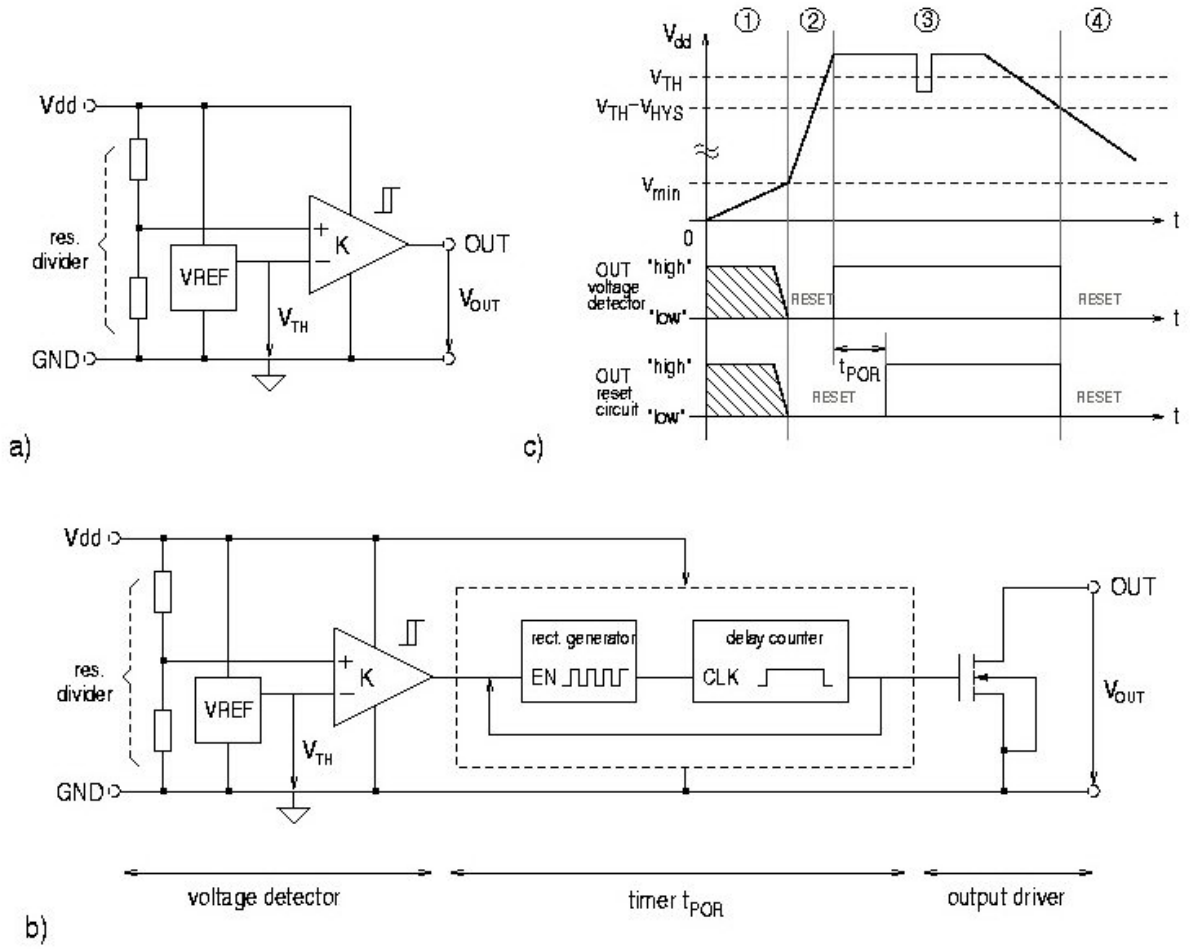

Figure 8. General supervisory architectures: a) voltage detector, b) reset circuit, c) timing waveforms of a and b.

The Architecture and Principle of Supervisory Circuits

This section deals with the principles and circuit architecture of supervisory circuits. Device parameters and features will be introduced further on that discuss both the bulk and SOI case of implementation.

Supervisory circuits act as smart power control units "supervising" the supply voltage of IC peripherals (microprocessor systems for instance). The main function of the supervisory circuit is to report the voltage decrease when power is going down. It is also responsible for generating a smart and safe reset signal for the connected IC peripherals.

The block architecture derived from the basic functional requirements is shown in Figure 8. In the simplest case, the system has only three pins. In this case the V_{dd} terminal performs the function of the supply voltage input, and the OUT terminal acts as a logical output to generate the appropriate RESET signal (note that all signals are related to the common ground, GND). Depending on the response of the output RESET signal, two types of supervisory chip architecture can be distinguished, the voltage detector (see Figure 8a) and the reset circuit (see Figure 8b). The principle and timing waveforms can be obtained from the schematic of 8c). The timing specification and circuit arrangement in this figure are simplified to emphasize the main idea.

Generally, the V_{dd} input monitors the supply voltage continuously and if $V_{dd} < V_{TH}$ occurs, the V_{OUT} signal goes to low (RESET). The decision is made by comparator *K* and voltage reference circuit V_{REF} generating the appropriate threshold value VTH. Both circuit variants — the voltage detector as well as reset circuit — have the same behavior model in the case where the supply voltage increase (see the time chart of V_{dd} within regions 1 and 2 of Figure 8c). Region 1 corresponds to

the initial operating phase of the device and will be discussed later. In region 3, the output time response is different in each case.

In voltage detector circuits, the reset is deactivated immediately after V_{dd} reaches the V_{TH} threshold value. In reset circuits reset occurs after a specific time delay t_{POR} given by additional timer block (see Figure 8b). Once the reset signal has been deactivated, its reactivation is possible only if V_{dd} drops below V_{TH} -V_{HYS}, where V_{HYS} is the value of comparator hysteresis (as seen in region 4, Figure 8c). Obviously, this solution improves the general noise immunity of the system (refer to the random rejection pulse within region 3, Figure 8c).

Another important parameter is the minimum guaranteed reset output voltage V_{min}. It is defined by the minimum V_{dd} voltage value needed for proper behavior of the logical output OUT. In region 1, Figure 8c, the power goes up from zero and the output is initially undefined (see the dashed lines in the time chart). However, the OUT pin should be in a correct logical state determined by input V_{dd} condition (=RESET), as soon as the supply voltage increases above V_{min} value. Note that this value depends on parameters of the target technology process used for circuit realization, as it will be explained in the next sections.

Supervisory Circuits — Bulk versus SOI

This section deals with parameters and features of typical production line supervisory circuits. Device parameter optimization will be discussed and significant trends of development will be demonstrated on supervisory products with parameters adjusted "to the upper limit" of the conventional technology processes. Such circuits are generally realized either on bulk as off-the-shelf products, or will be soon available on SOI as the upcoming solution. The parameters are taken from [8 - 10].

Important Circuit Parameters

Current consumption - Since the supervisory circuit is often part of a battery operated system, it is importance to reduce its current consumption as much as possible.

Static current consumption becomes dominant in the analog parts of the system, such as V_{REF} circuit, comparator, and other parts where specific values of bias currents are needed to ensure the correct function. The current bias value needed for biasing of voltage reference circuit significantly contributes to the total current consumption. This is due to the fact that conventionally, a bandgap circuit concept is used for the VREF circuit realization. In bandgap designs, the static current consumption cannot be much lower than a few microamps. The reason is that sufficient biasing current must be applied to both diode sections to ensure correct behavior of the bandgap loop[11].

Difficulties can be encountered while realizing bandgap circuitry in conventional CMOS processes; namely, performance can be degraded by low values of the bipolar gain, provided by the lateral bipolar structures available in standard CMOS. The situation is much worse in SOI CMOS where bipolar transistors with gains of =10 can be fabricated. This is a natural consequence of the higher latchup immunity of SOI, making bipolar device creation more difficult. To improve the bandgap properties, several sophisticated solutions such as the beta-helper circuits[11] have been developed.

However, to significantly reduce the power consumption of voltage reference circuits, another circuit concept called "threshold voltage difference" seems to be more reasonable. The principle is based on subtraction of the threshold voltage values of two MOS devices with various gate doping profile[12]. The bias current value forcing the transistors can be very low, deep in sub-threshold device region and comparable with the typical value of structural leakage currents. Thanks to lower SOI device leakage, SOI technology becomes advantageous with the realization of ultra low power voltage reference circuits achieving power consumption, even at pA level.

Dynamic current consumption creates the second part of the total power dissipation equation. Referring to the block arrangement of the supervisory circuit in Figure 8b, the voltage detector enclosing the comparator and voltage reference circuit is, in fact, a statically operated two-state circuit. Therefore its dynamic consumption does not play a significant role. Thus in the following text, the digital part containing the rectangular generator and delay counter will be discussed.

These circuits are predominantly built on standard digital cells such as logical gates and elementary sequence logic (counters, flip-flops, etc.) For dynamic current consumption, the reduced area of source and drain junctions of MOS devices built on SOI helps to achieve lower leakage current. And the reduced source-drain capacitance helps to achieve lower active (saturation) current compared to bulk[11] (see Table 1 - parameter ID_{sat}), and the section on the SOI advantages for use in LP-LV systems. Generally, one can expect about a 50% reduction in current consumption of SOI digital circuits and standard cells[11]. Furthermore, capacitance reduction also leads to higher speed of SOI digital circuits (reduced delay and access time of about 25%).

Supervisory Threshold and Guaranteed Output Voltage

The range of supervisory threshold voltage (parameter V_{TH} in Table 1) also depends on the threshold voltage value of the MOS devices available for circuit fabrication. The lower the MOS device threshold, the lower the V_{TH} of a supervisory circuit. The device threshold is potentially lower in SOI (see Table 1) and therefore very small V_{TH} values (below 1 V) can be designed (see Table 1). A lower MOS threshold voltage also has a positive impact on another supervisory parameter; guaranteed output voltage — V_{min}.

This parameter is determined by both the minimum supply voltage for digital circuits (t_{POR} timer — Figure 8b) as well as the threshold voltage of MOS devices used in the analogue part (voltage detector). Therefore, lower values of V_{min} can be expected with SOI than bulk (see Table 1).

The upper bound of supervisory threshold voltage is affected both by achievable MOS device breakdown and by the quality and performance of ESD circuit protection. The upper bound of supervisory threshold voltage is affected both by achievable MOS device breakdown voltage and by the quality and performance of ESD circuit protection. Unfortunately, the device breakdown voltage on SOI (see parameter B_{VDS} in Table 1) might be lower than bulk in some cases. The reason is parasitic bipolar structure with floating base present in non-optimized SOI MOS transistors[3].

Even though sophisticated techniques, such as LDD have been invented, the breakdown voltage of the current SOI technology does not allow the development of supervisory circuits with higher threshold voltage values. Therefore, SOI is predominantly dedicated for use in low voltage supervisory circuits.

Operating Temperature Range

SOI technology becomes a prime candidate for implementation in robust and hardened circuits for high-temperature operation. Therefore, the temperature operation range given in Table 1 could be much wider, enabling the circuit to operate in extreme conditions. However, the implementation of high temperature option to supervisory circuit design is still in largely developmental.

Conclusion

This article has presented a perspective on SOI — one of today's most promising technologies for semiconductor fabrication. The main aim was to introduce the basic features of SOI technology and compare it to conventional bulk processes. The discussion focused on SOI device properties for LP-LV operation, which is a significant trend of modern circuit development. Supervisory circuits were highlighted as a promising start to a new era of further SOI development.

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Glossary of Acronyms

CMOS - Complimentary Metal-Oxide Semiconductor
GAA - Gate-All-Around
IC - Integrated Circuit
LDD - Lightly Doped Drain
LP-LV - Low-Power, Low-Voltage
MOSFET - Metal-Oxide Semiconductor Field-Effect Transistor
PD - Partially Depleted
SOI - Silicon-On-Insulator

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