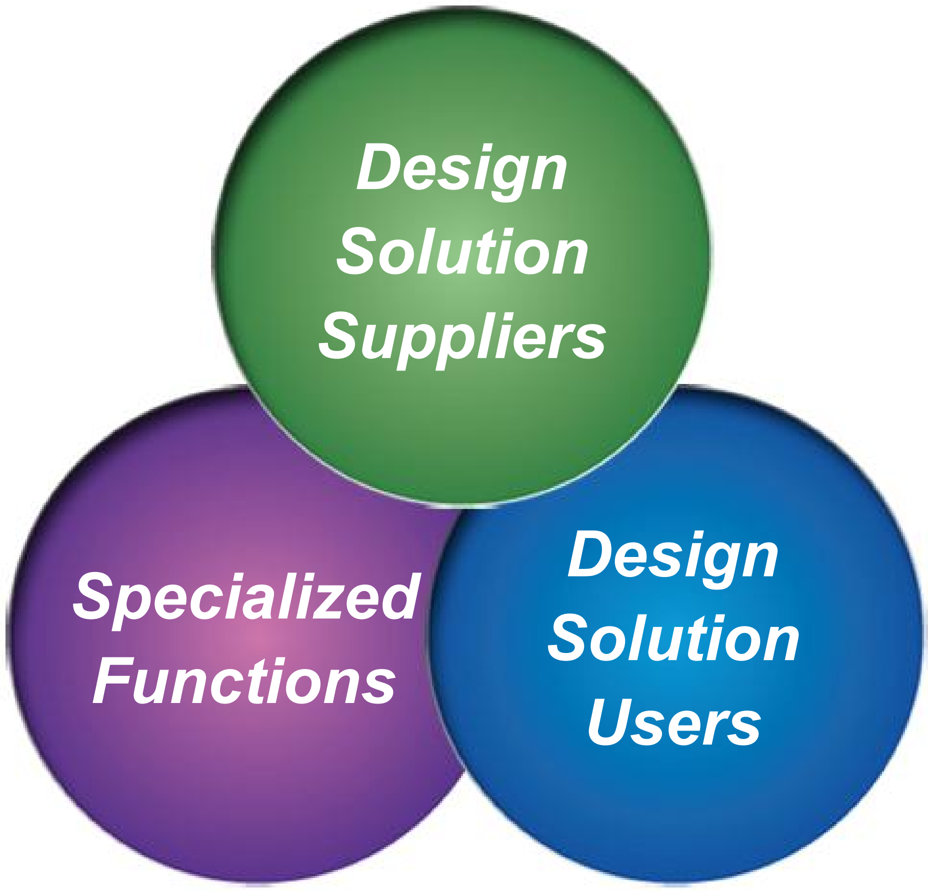
Sociology of Design and EDA

March, 2006

Walden C. Rhines
CHAIRMAN & CEO

Mentor Graphics®

Electronic Design Automation (EDA)- A Perplexing Ecosystem



Electronic Design Automation (EDA)- A Perplexing Ecosystem

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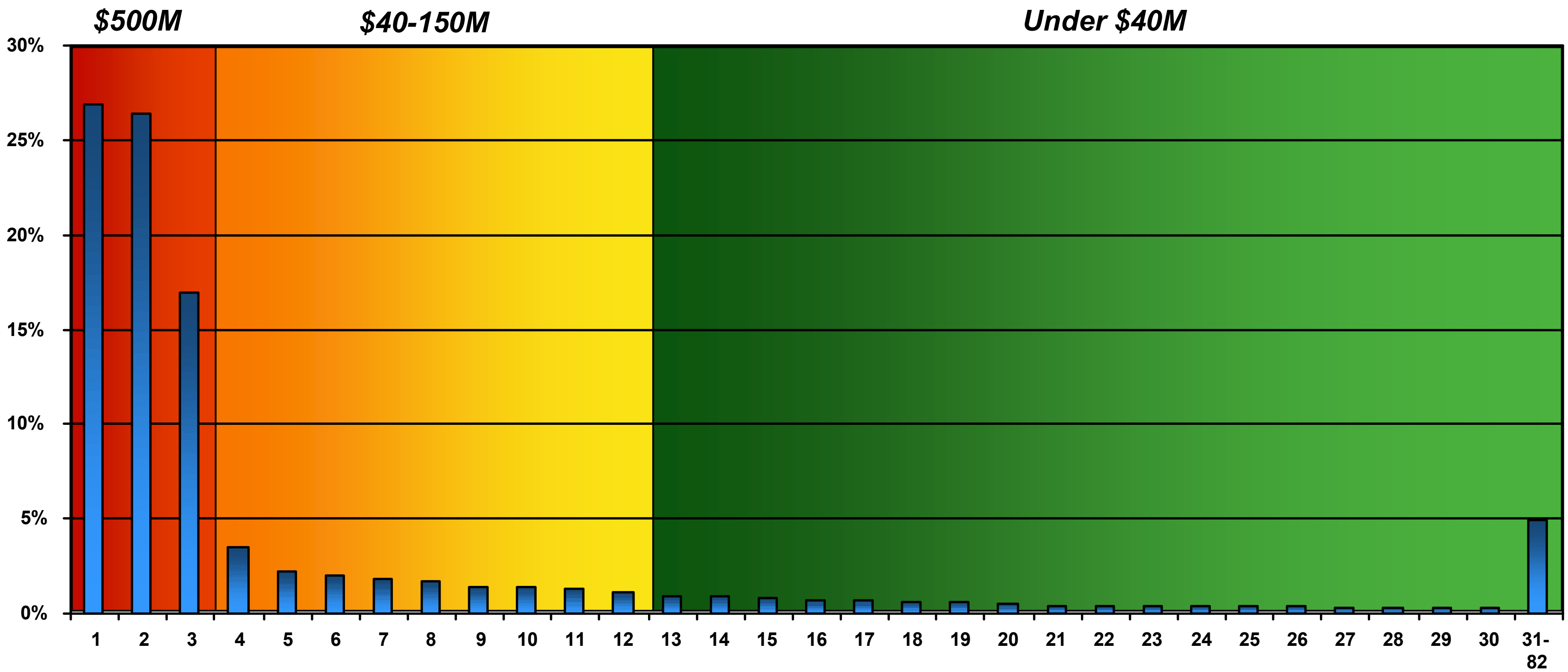
"Big 3" Have About 75% Market Share…



$500M +	**(Big 3) Cadence, Synopsys, Mentor Graphics**
$40M to $150M	**Small Public Companies (Magma, ARM, Agilent EEsof, Zuken, Verisity*, Synplicity, Ansoft, i2, Nassda*)**
Under $40M	**Niche, regional and start-up companies**

Source: Gartner/Dataquest Market Share Report
**Versity acquired by Cadence; Nassda acquired by Synopsys*

The Hidden World of EDA

<u>EDA Company Lists</u>

Gartner/Dataquest companies published …………….	82
DAC Exhibitors …………………………………………….	184
DATE Exhibitors ………………………………………….	74
EDAC Voting Members …………………………………..	101
EDA Café PCB Design …………………………………..	8
Printed Circuit Board List ………………………………	76

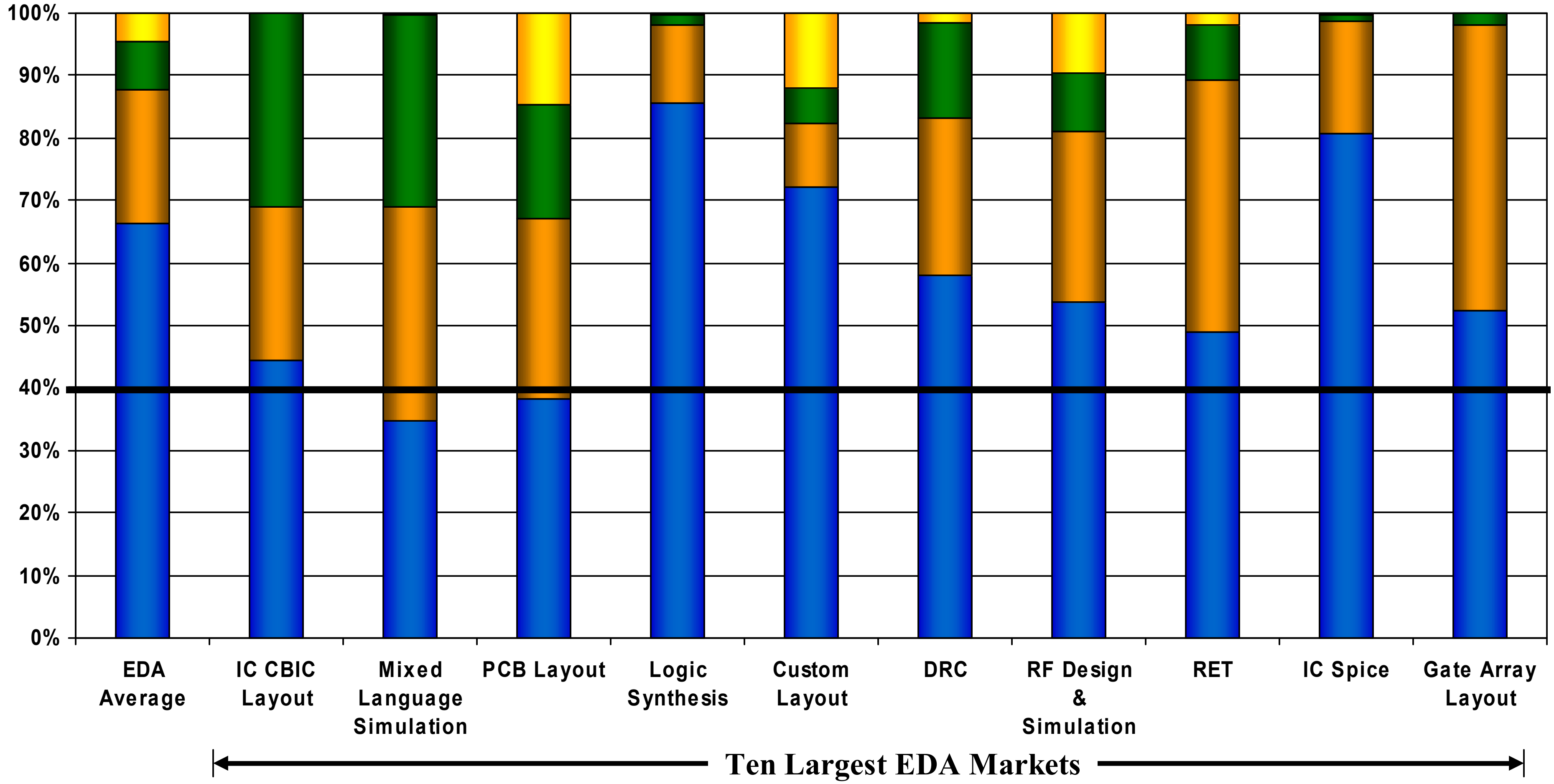
Eliminated: Platform Vendors, IP Companies, Consulting Firms, Consortiums, Publishers

Unique EDA Companies (Duplicates Removed) ………. 300

PLUS

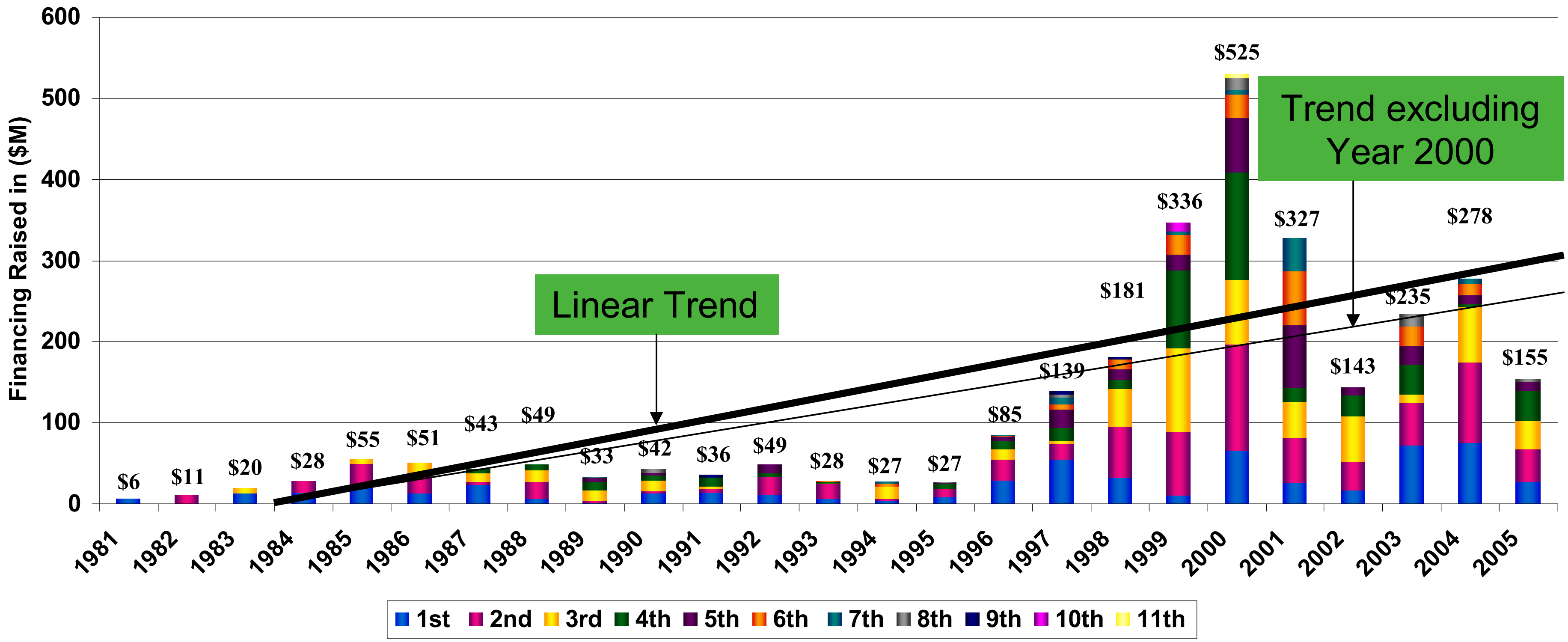
Many more niche and regional EDA companies

Product Leaders Average 66% Market Share



Source: Dataquest Market Trends, 12/05

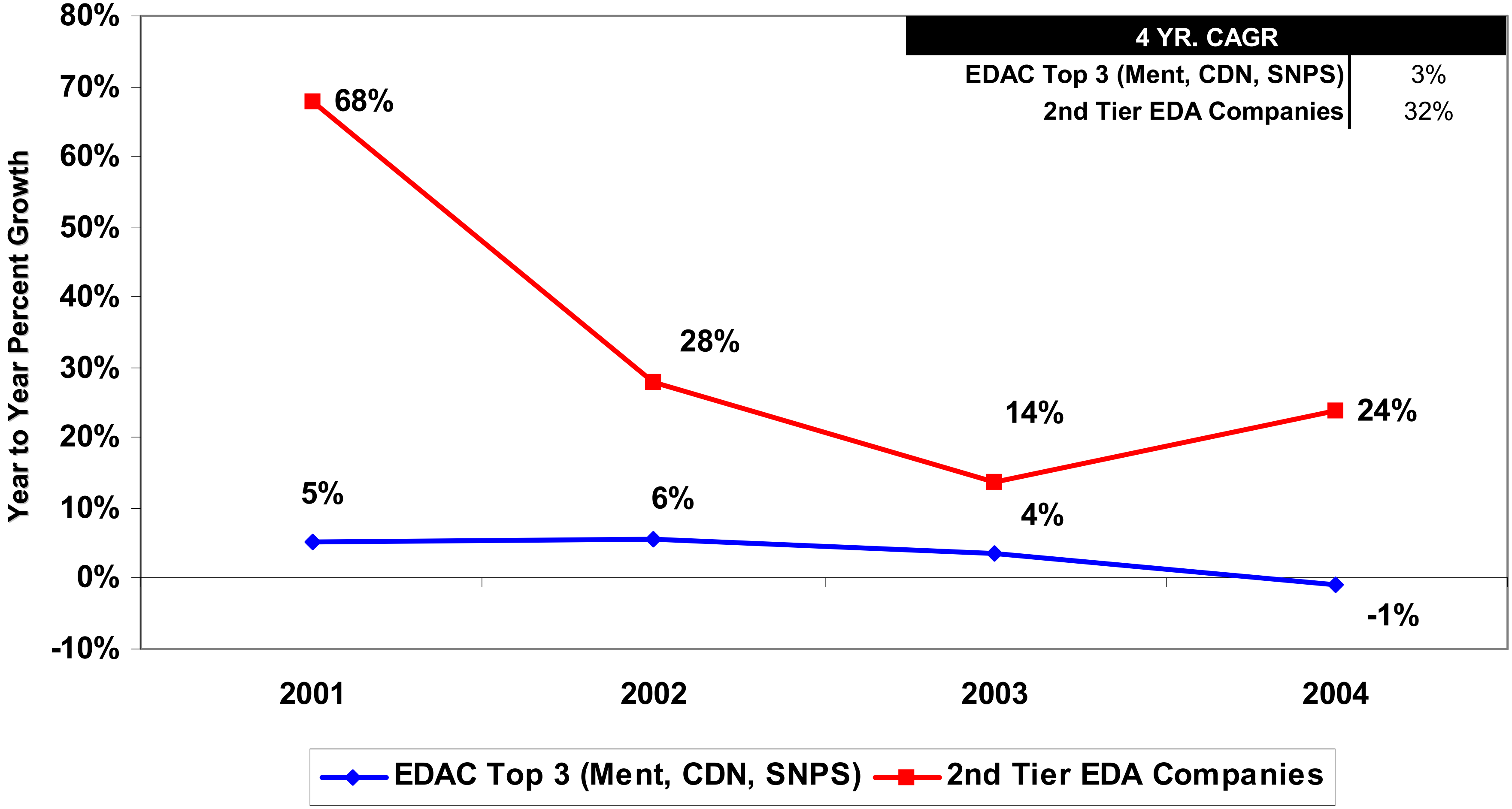
EDA Equity Financing per Year *(By Round – Excluding IPO's)



***Note:** Excludes round of funding in which (28) startups IPO'd & became public

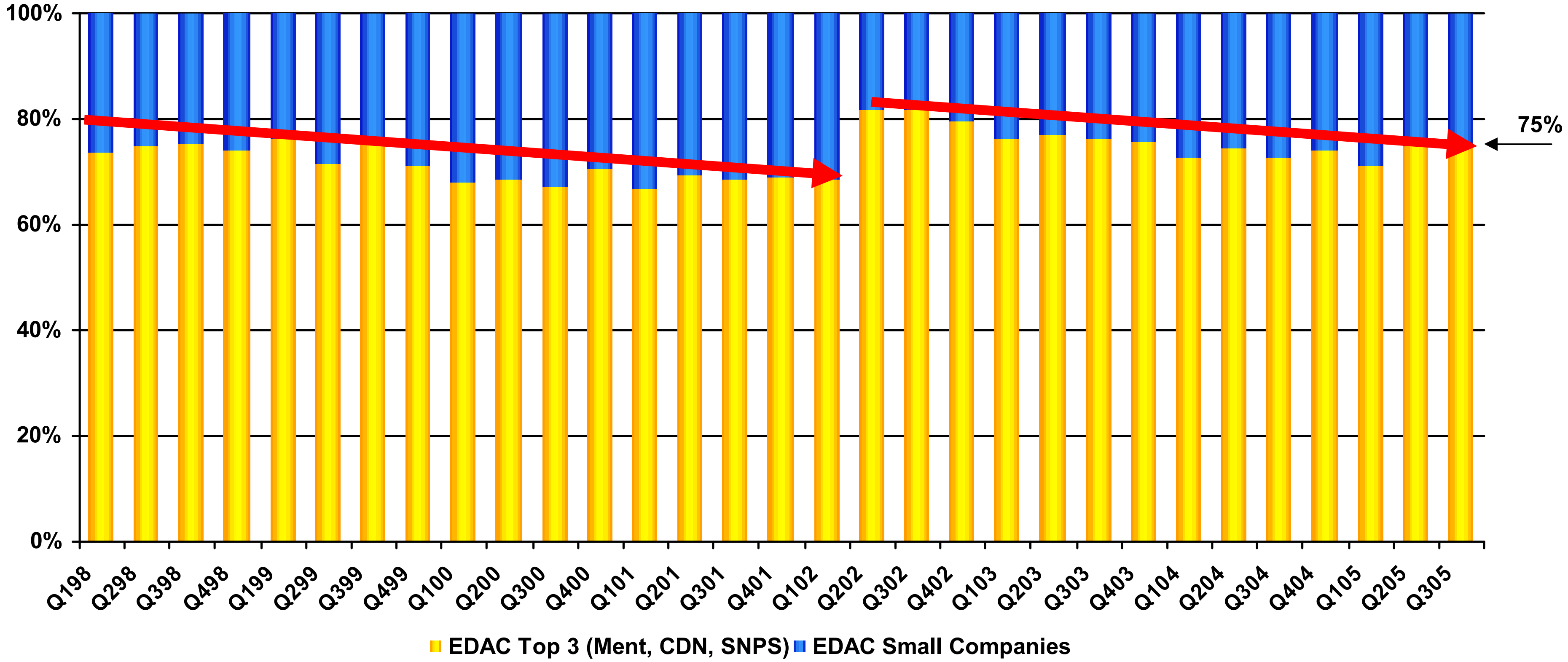
Source: VentureOne/Ernst & Young, EETimes, Company web sites

2nd Tier EDA Companies Grow Faster than the "Big 3"



Source: EDAC MSS, SEC and Annual Reports 2nd Tier EDA: Magma, Logic Vision, Nassda, Verisity, Virage Logic, Ansoft, Artisan, Synplicity

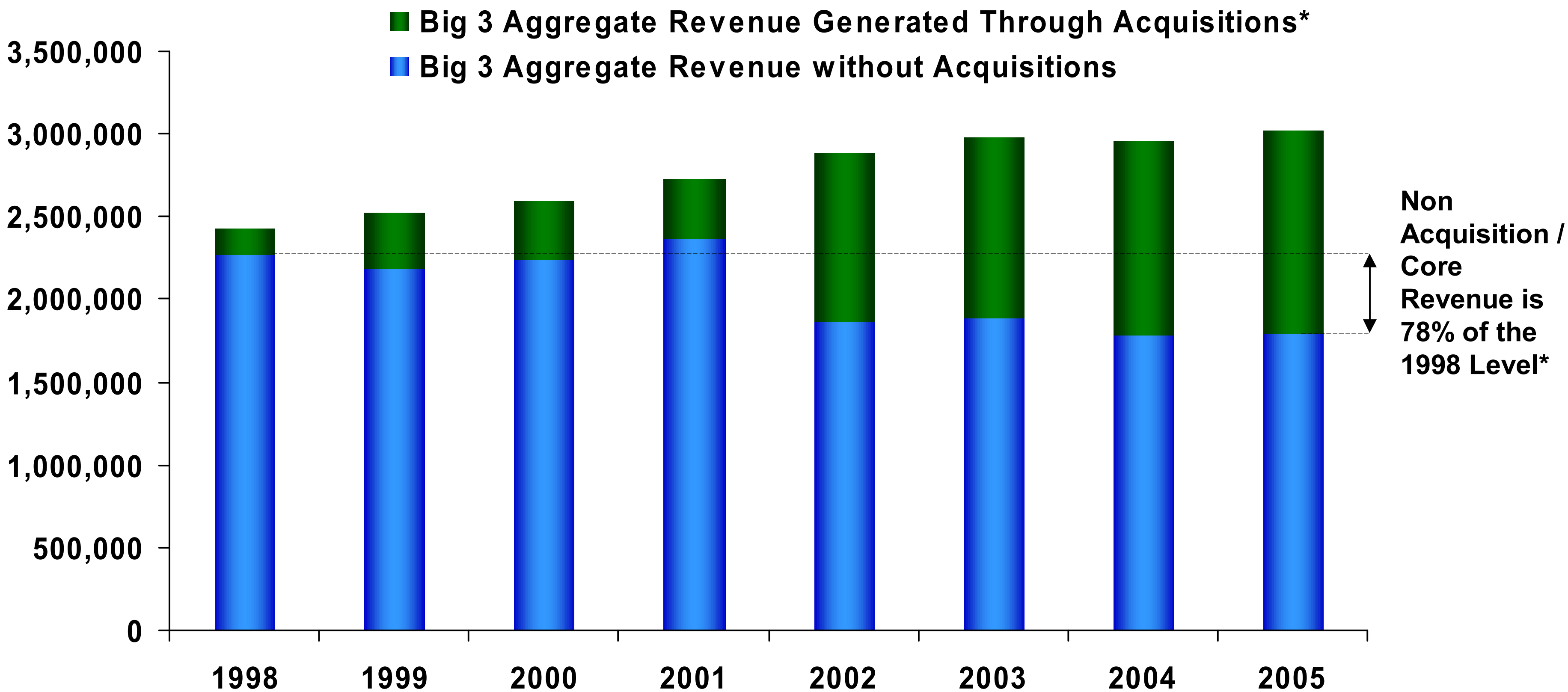
Acquisitions Sustain "Big 3" Market Share



EDAC Market Statistics Service
EDAC Revenue Analysis (Top 3 vs. All Others)- Excluding Non-Reporting SIP Companies -

Mentor Graphics

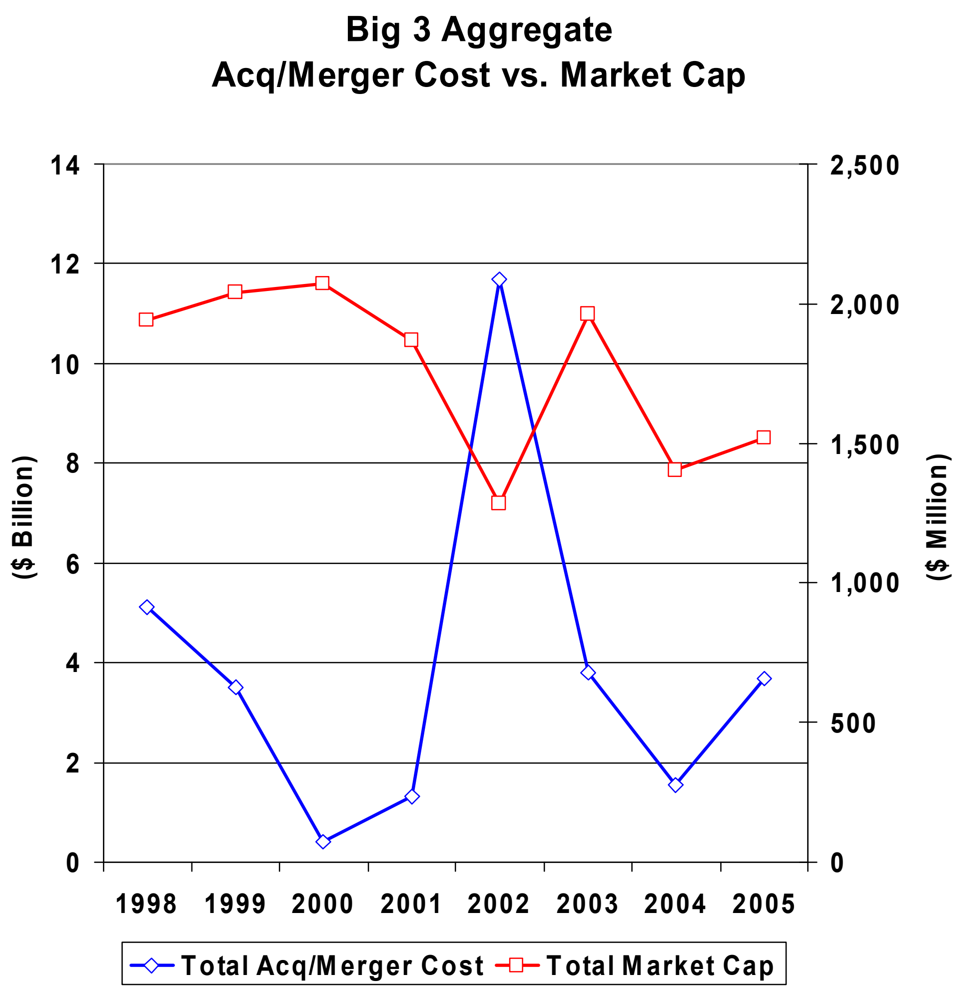
What If There Were No Acquisitions by the "Big 3"?

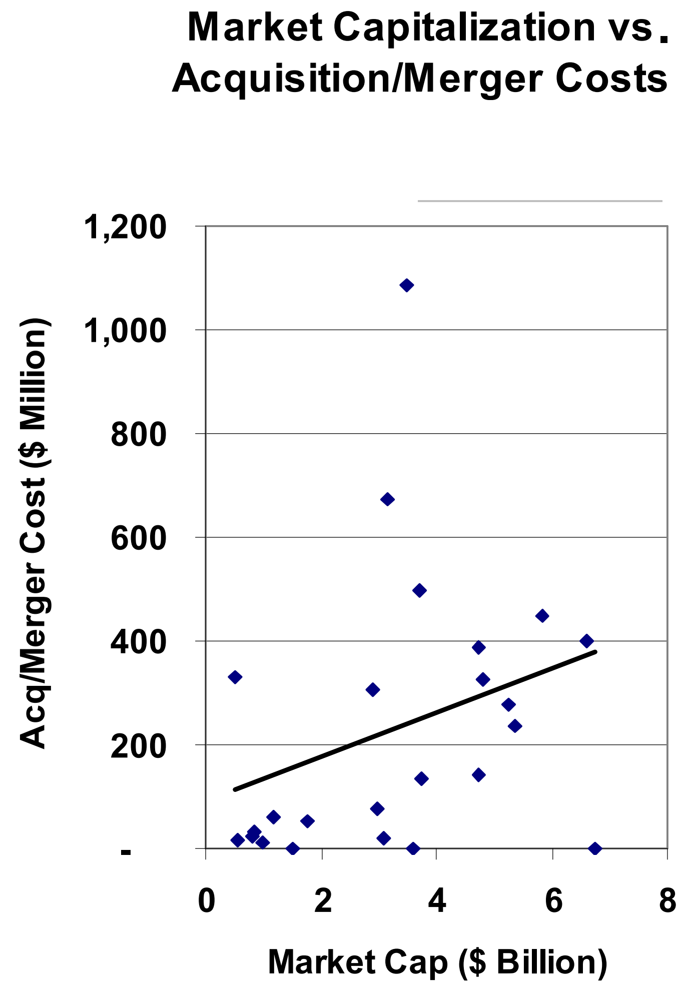


Source: Company Annual Reports, Gartner DQ, SEC and Mentor Graphics Analysis

**BIG 3: Mentor, Cadence, Synopsys. Acquisition revenue estimate based on run rate of acquired company; rate held constant. Data incorporated as available.*

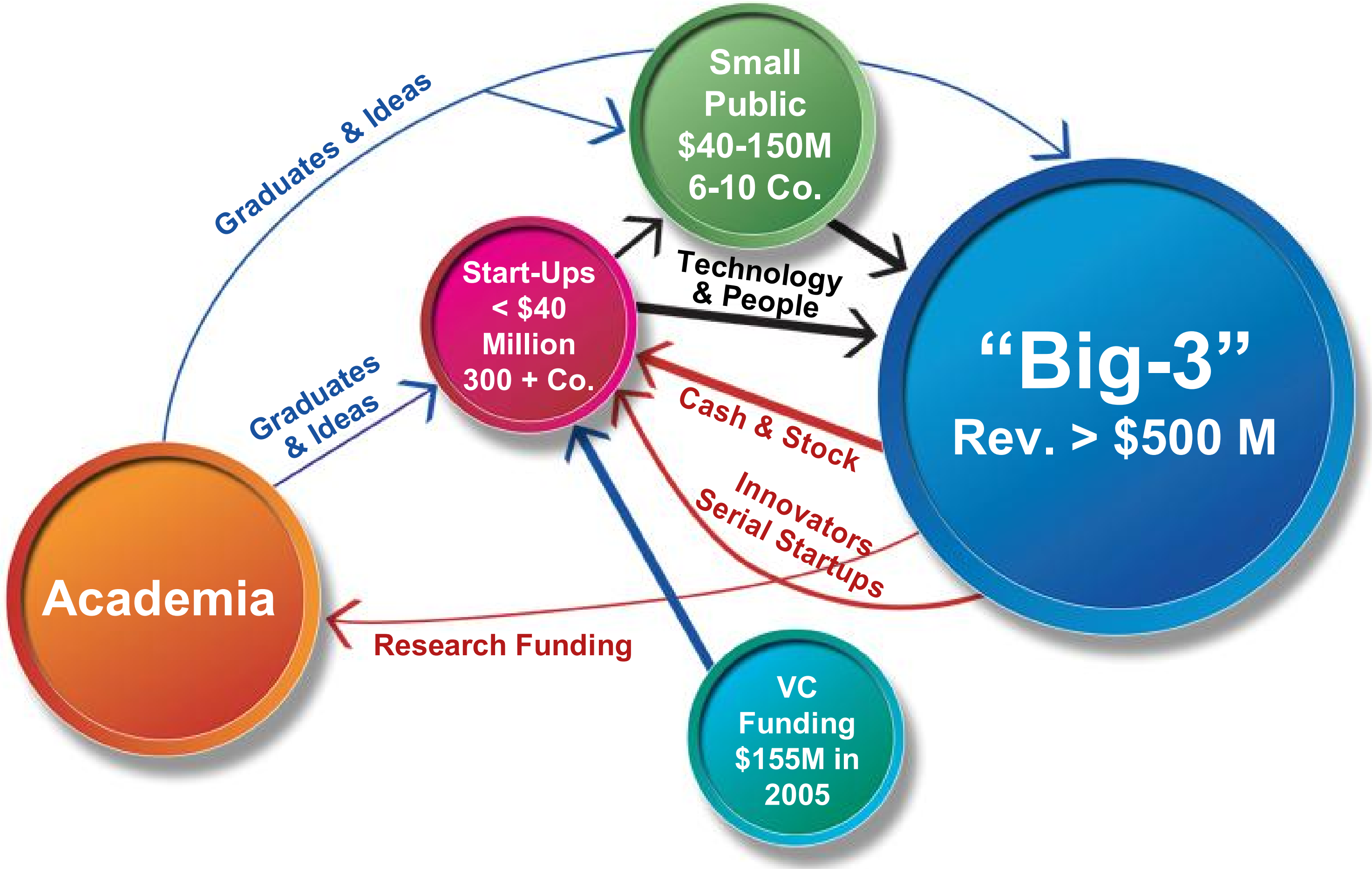
Market Capitalization vs. Acquisition Costs



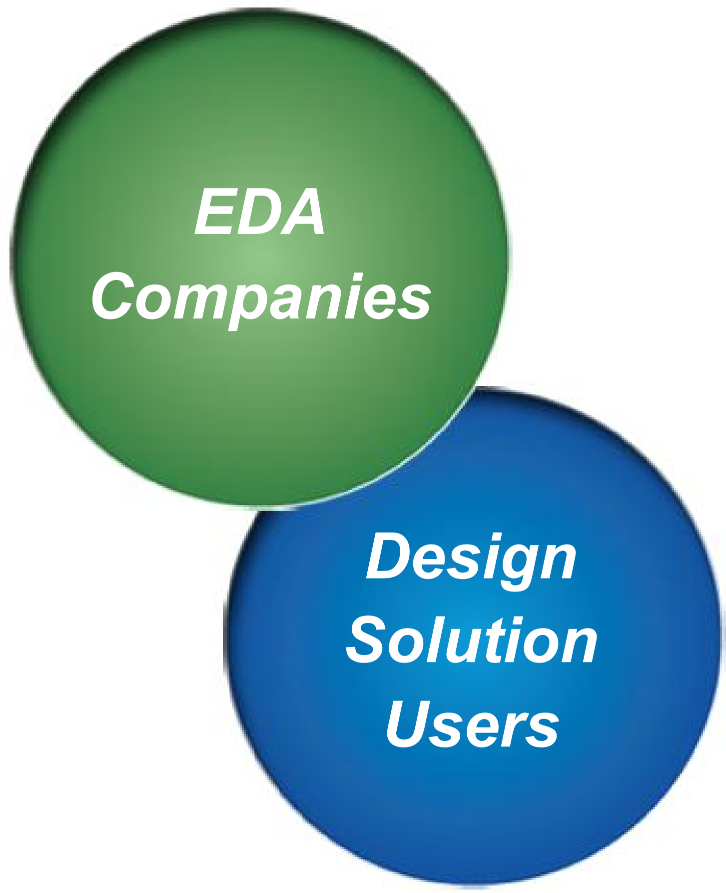


Source: Financial Reports, Company Press Releases, EETimes, Business Journal, Other Journal Resources

Circular Dynamic Between "Big 3" and Start-Ups (2000-2005)



Electronic Design Automation (EDA)- A Perplexing Ecosystem



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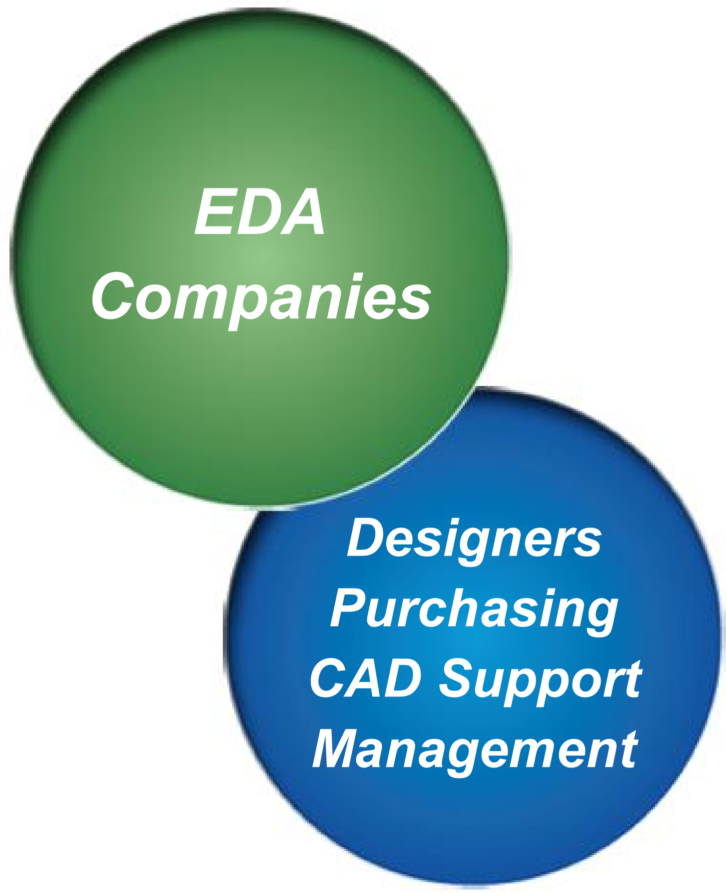
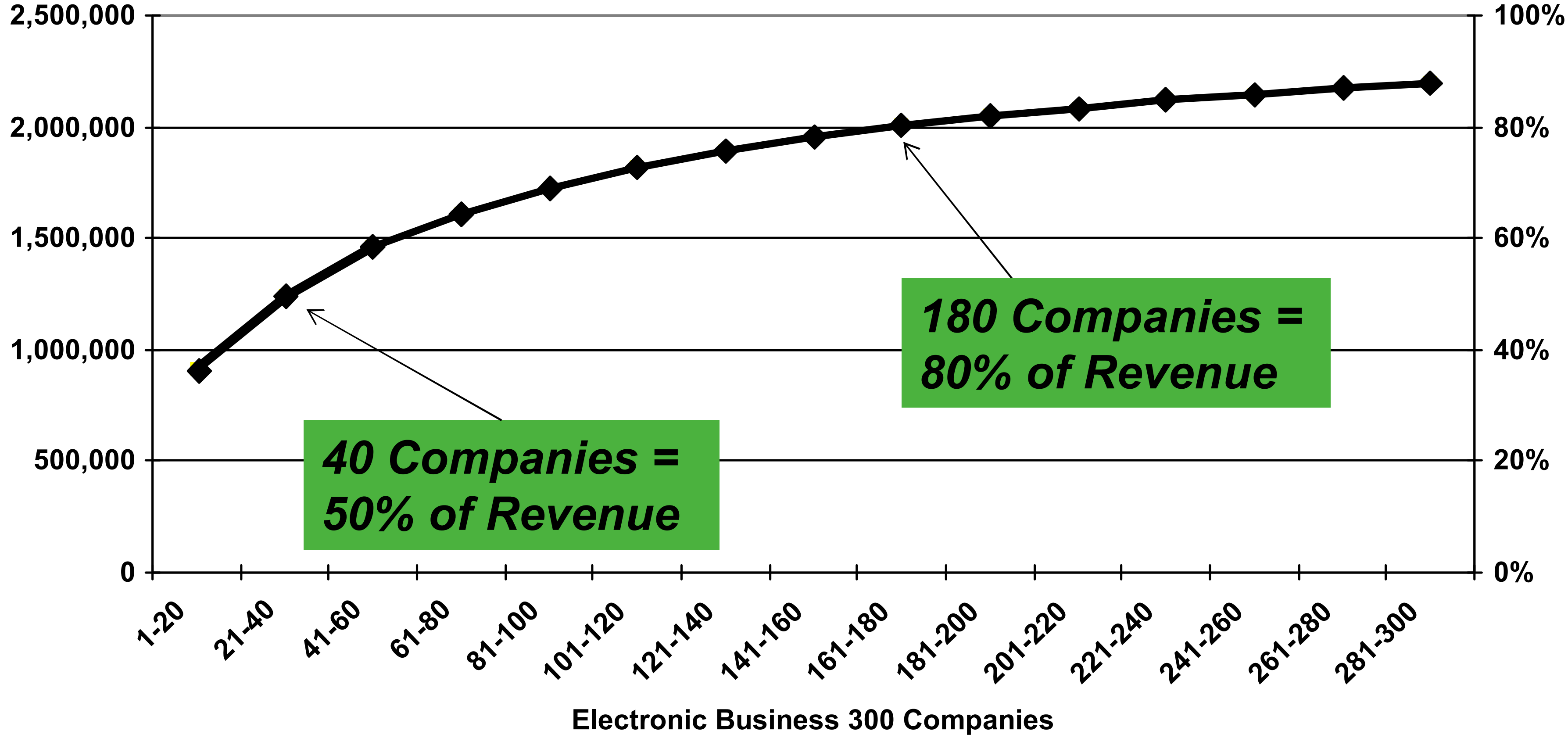
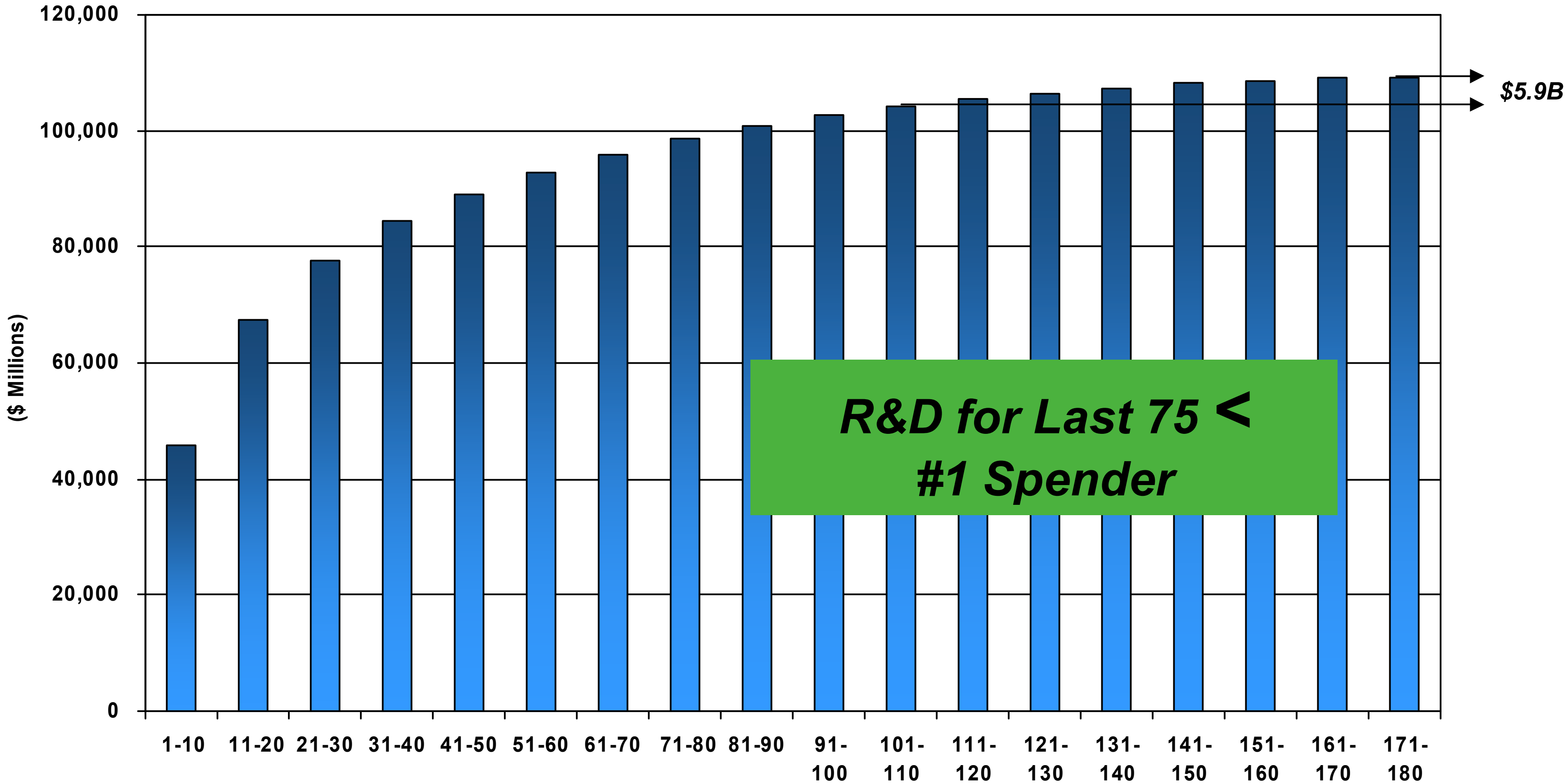


Electronics Revenue Concentration



Source: Reed Research Group – Electronic Business, 8/1/2005

Concentration of R&D Expense

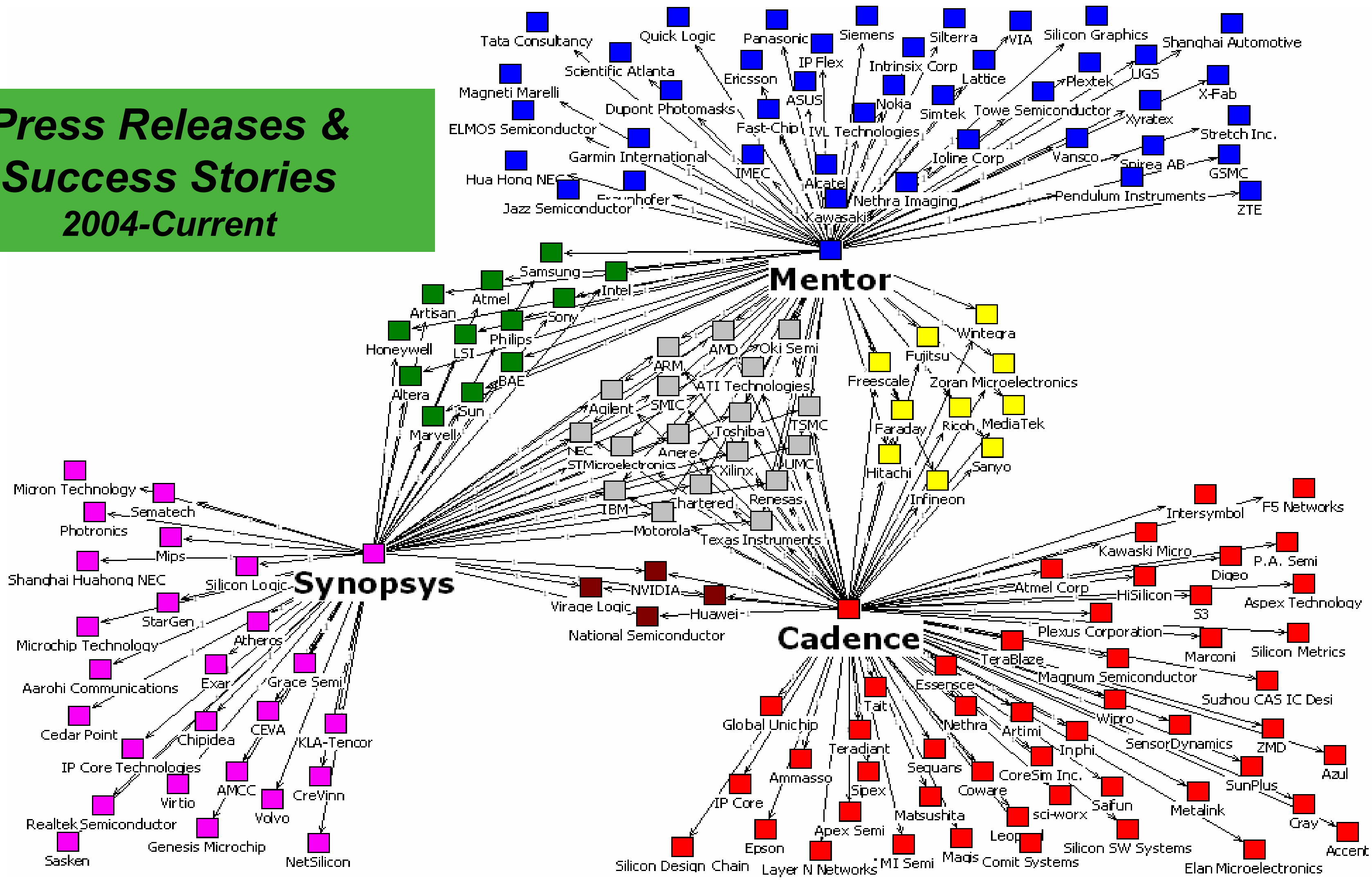


Note: Top 180 companies from EB 300 List with R&D data available and published, Software & Services companies excluded
Source: Reed Research Group – Electronic Business, 8/1/2005

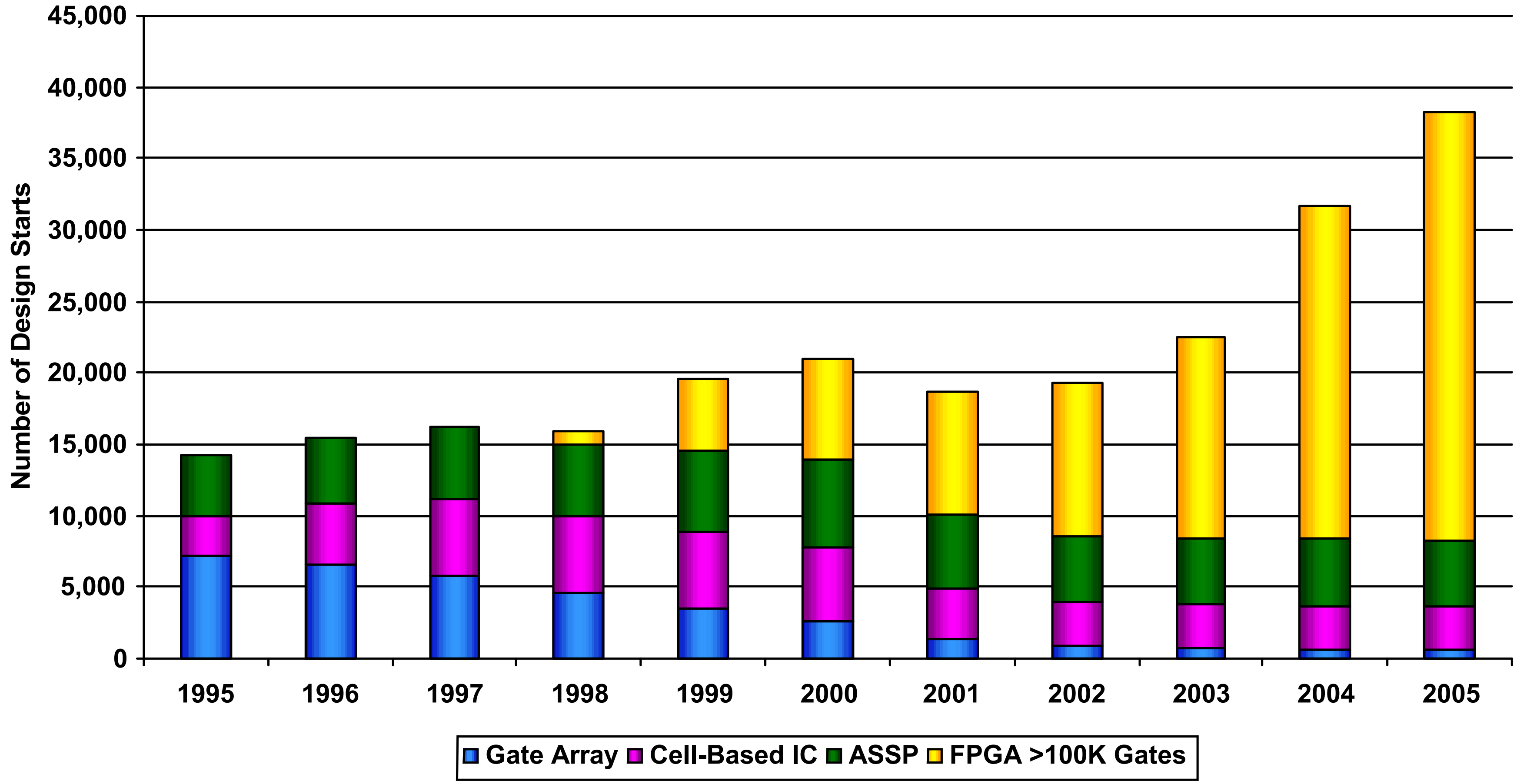
Fishing from a Limited Pool of Users

Press Releases & Success Stories

2004-Current



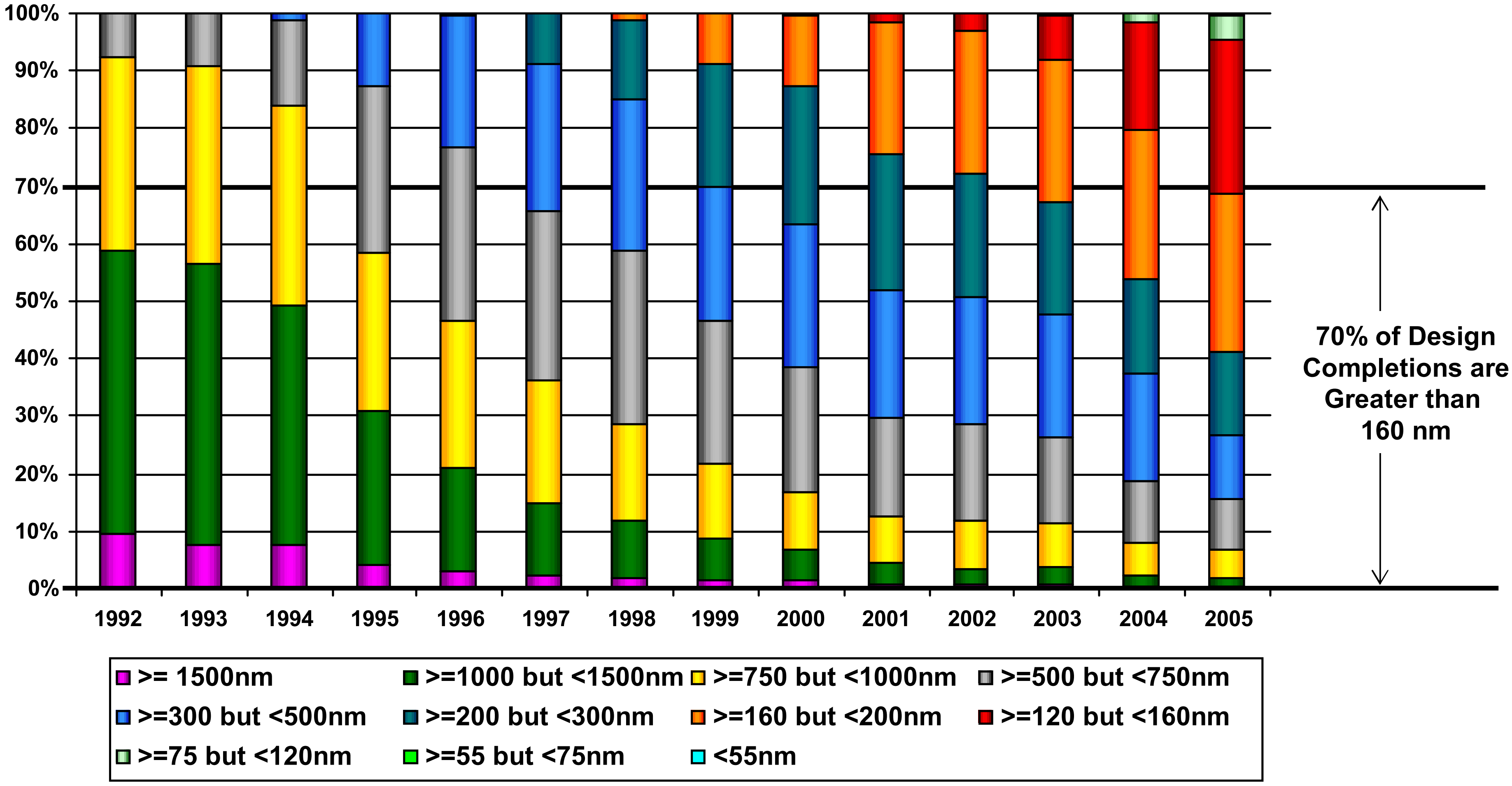
Worldwide Design Starts



Source: Gartner/Dataquest ASIC Market Trends …. FPGA Estimate based on Gartner/Dataquest ASIC Market Trends & User Surveys

Worldwide Design Completions

(by Drawn Line-width)



Source: VLSI Research, Worldwide Design Completions, 2006 …. Used with permission

Diverse Requirements for EDA Solutions

DESIGN

•Reliability •High Performance • Ease of Use • Functionality • Design Cycle Time

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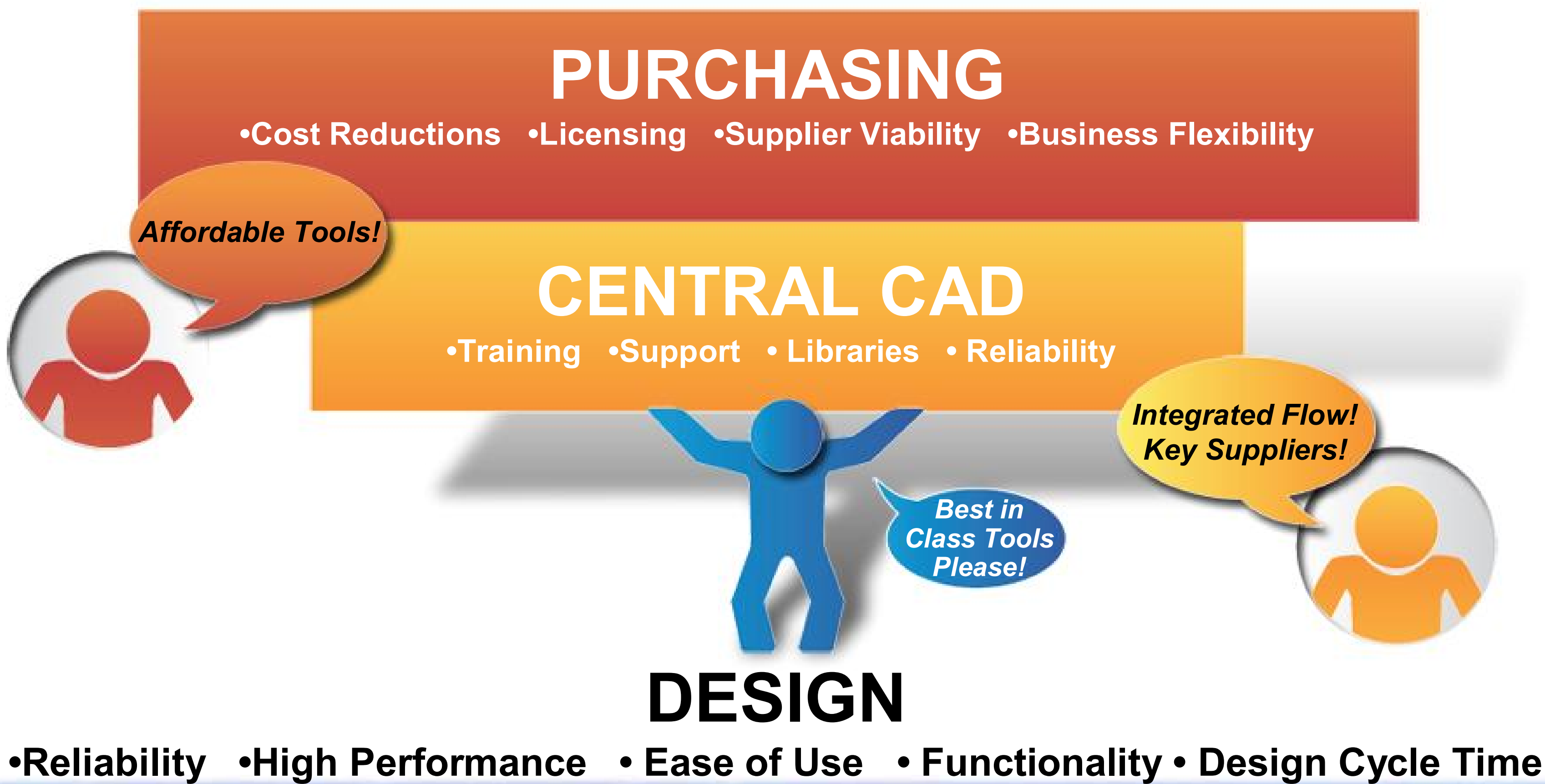
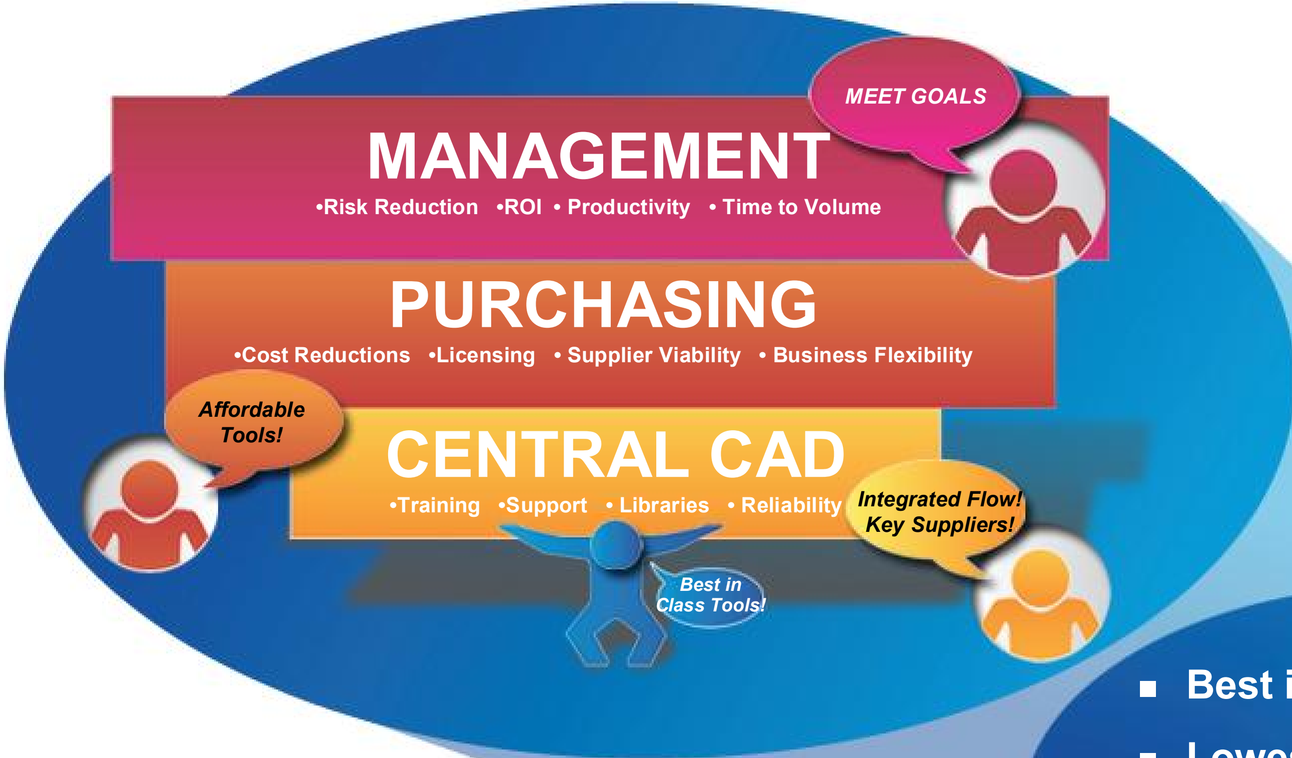
Diverse Requirements for EDA Solutions



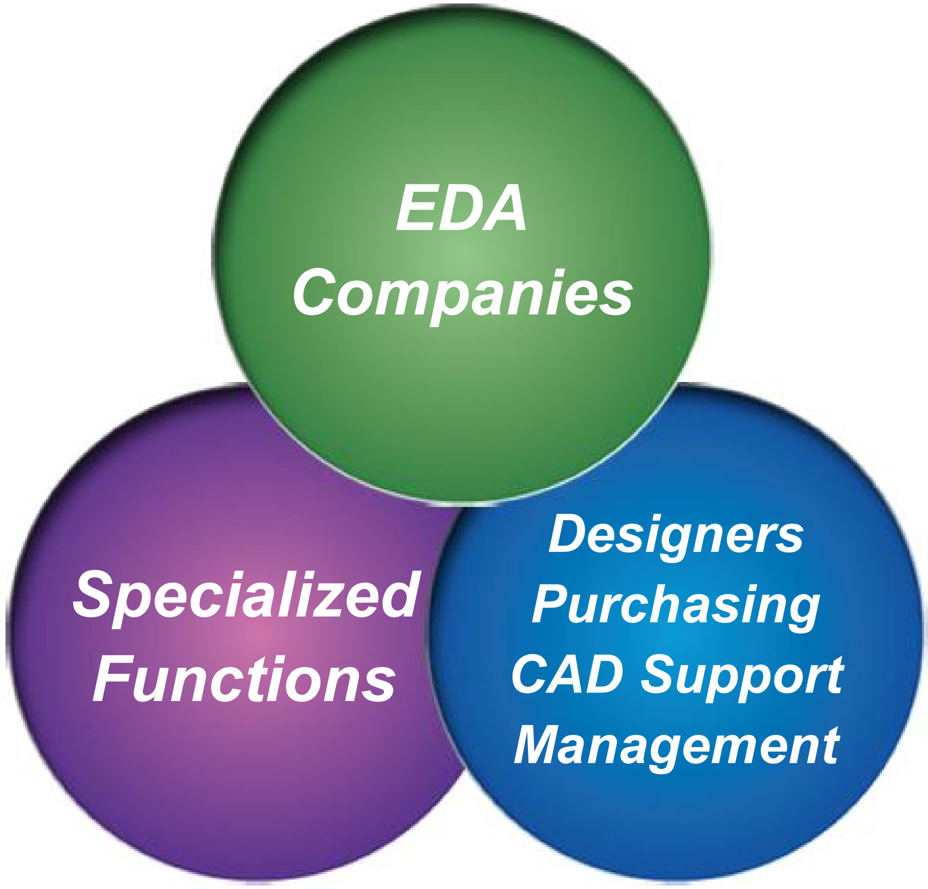
Diverse Requirements for EDA Solutions

Diverse Requirements But Common Goals



- Best in Class Design Tools
- Lowest Possible Cost
- Highest Reliability
- Low Infrastructure Cost and Time

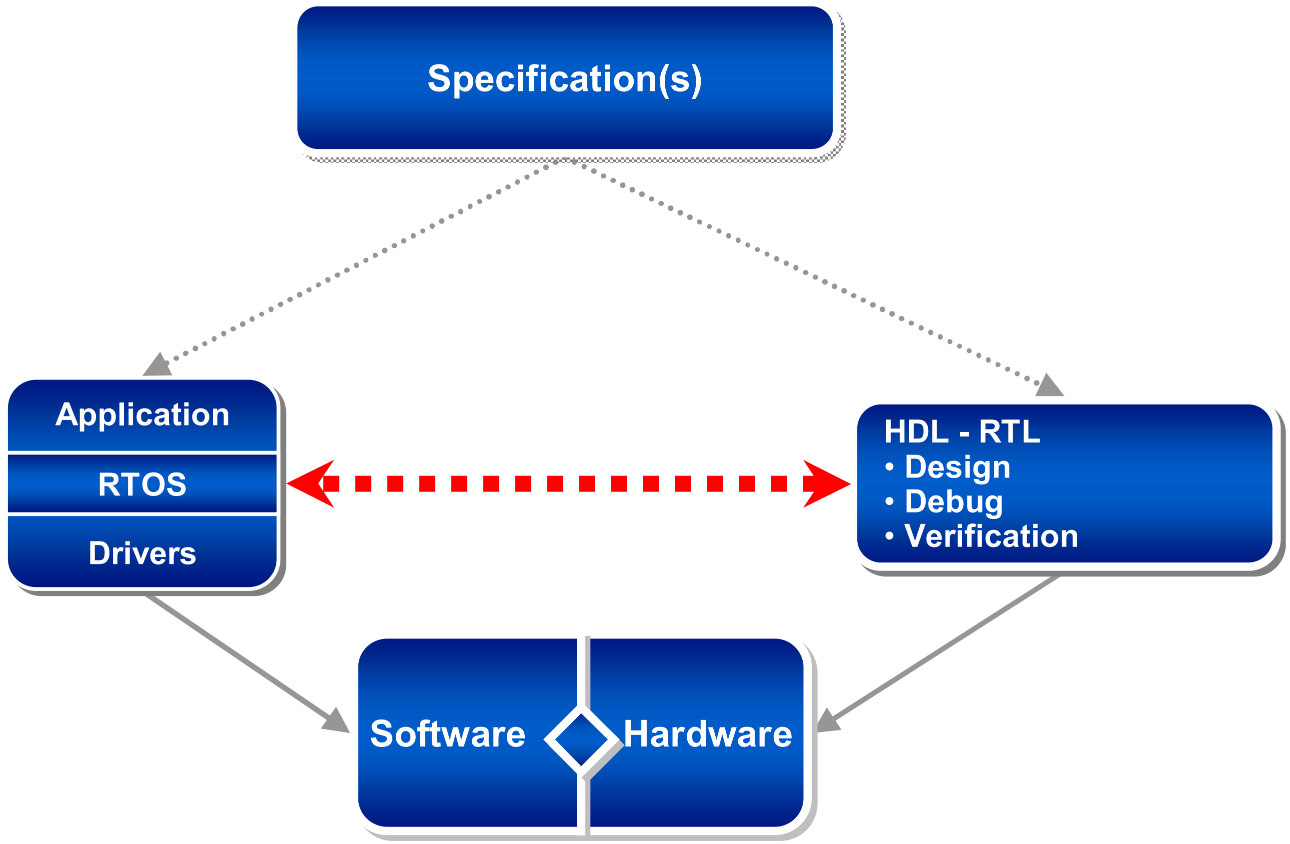
Electronic Design Automation (EDA)- A Perplexing Ecosystem



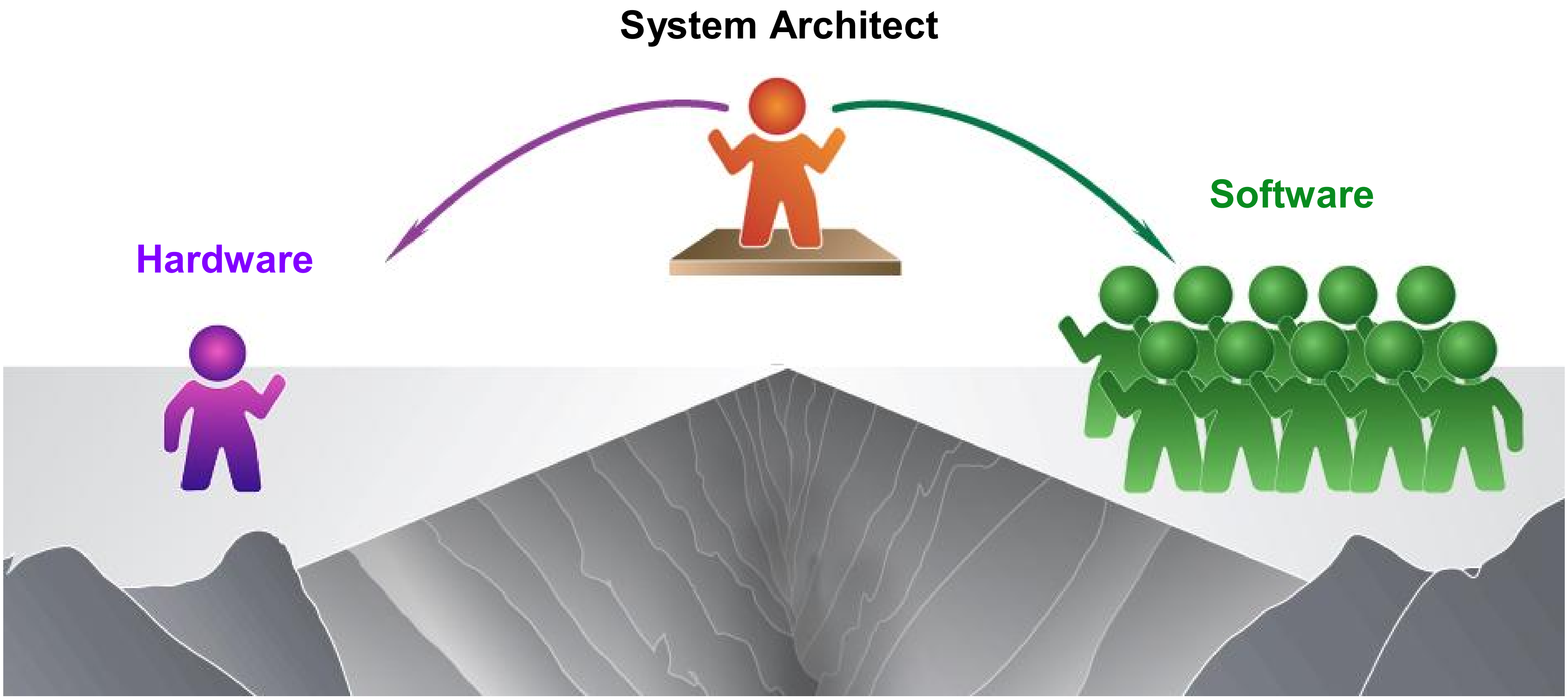
Sociology of Specialized Product Development Functions

- **Hardware vs. Software**

“Traditional” Hardware Software Flow

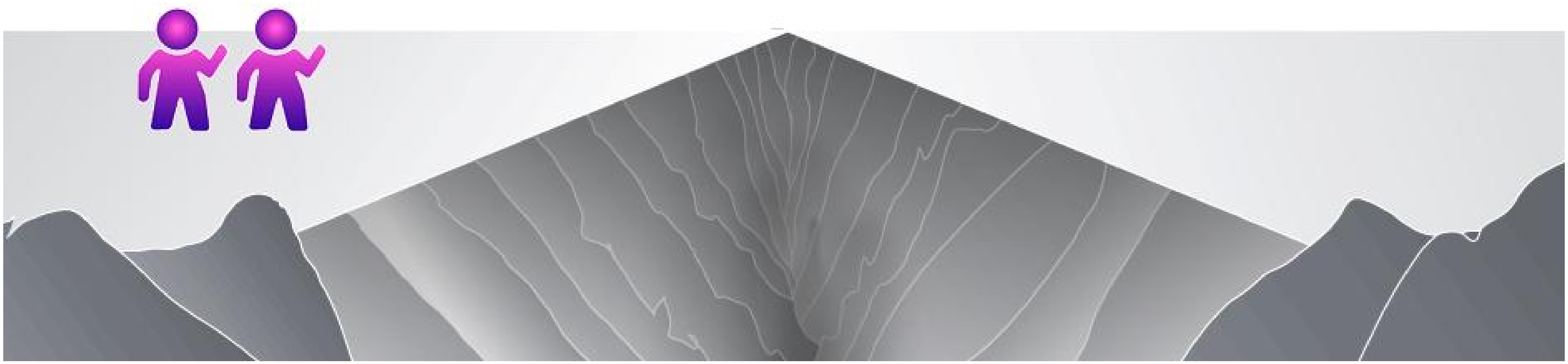


Hardware vs. Software

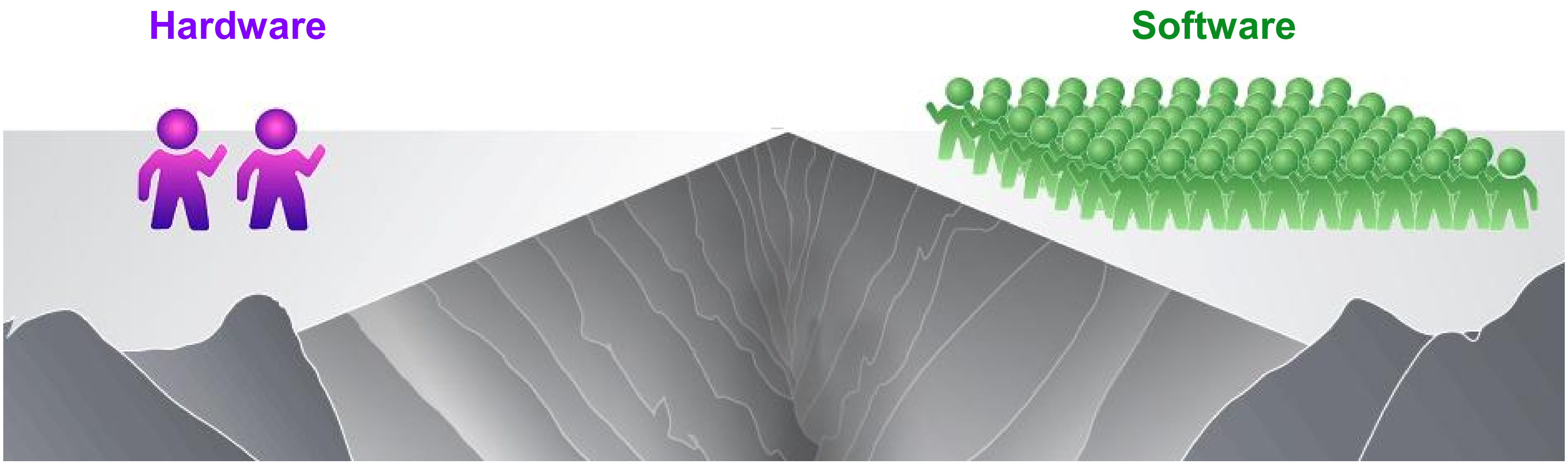


Hardware vs. Software

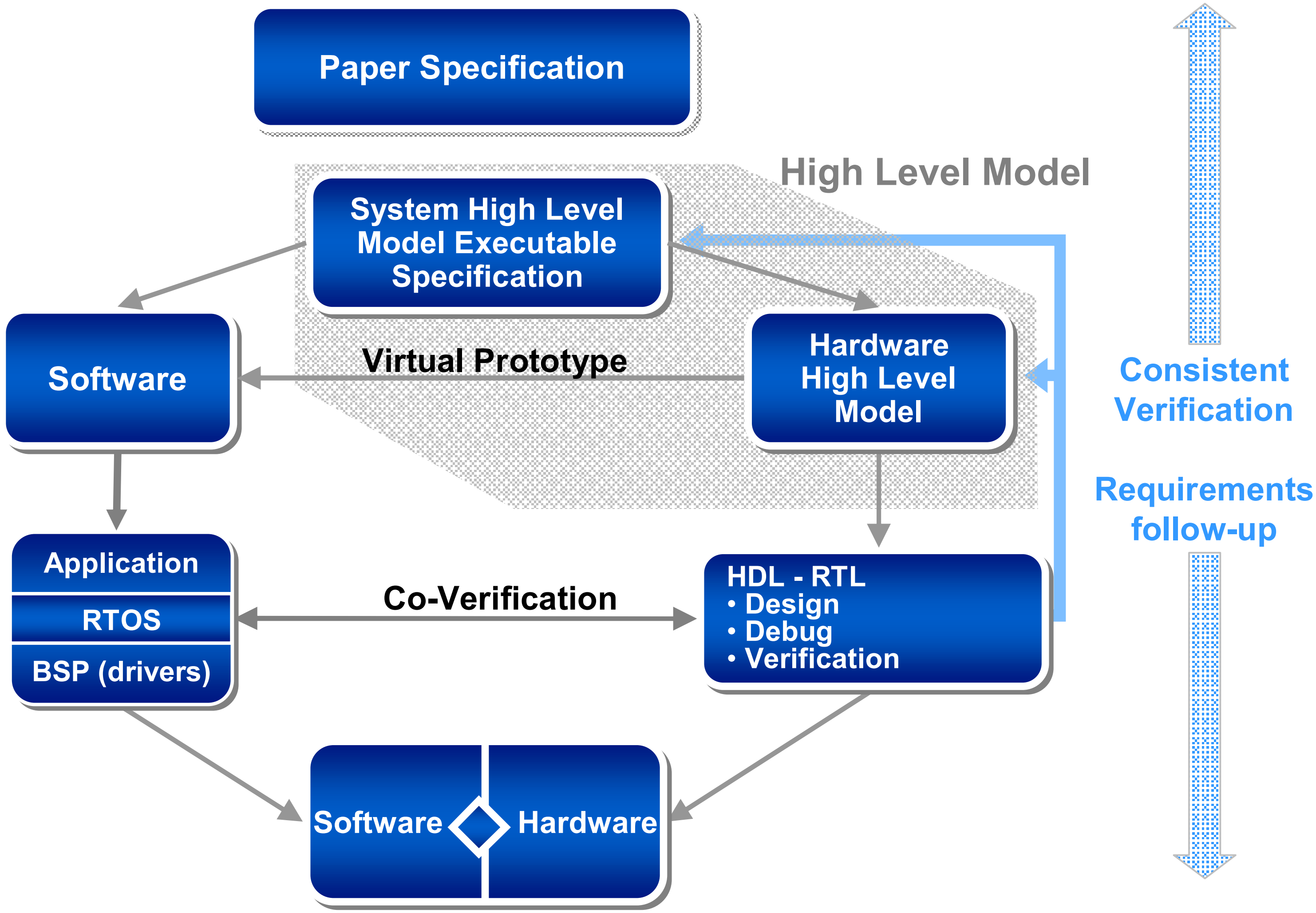
Hardware



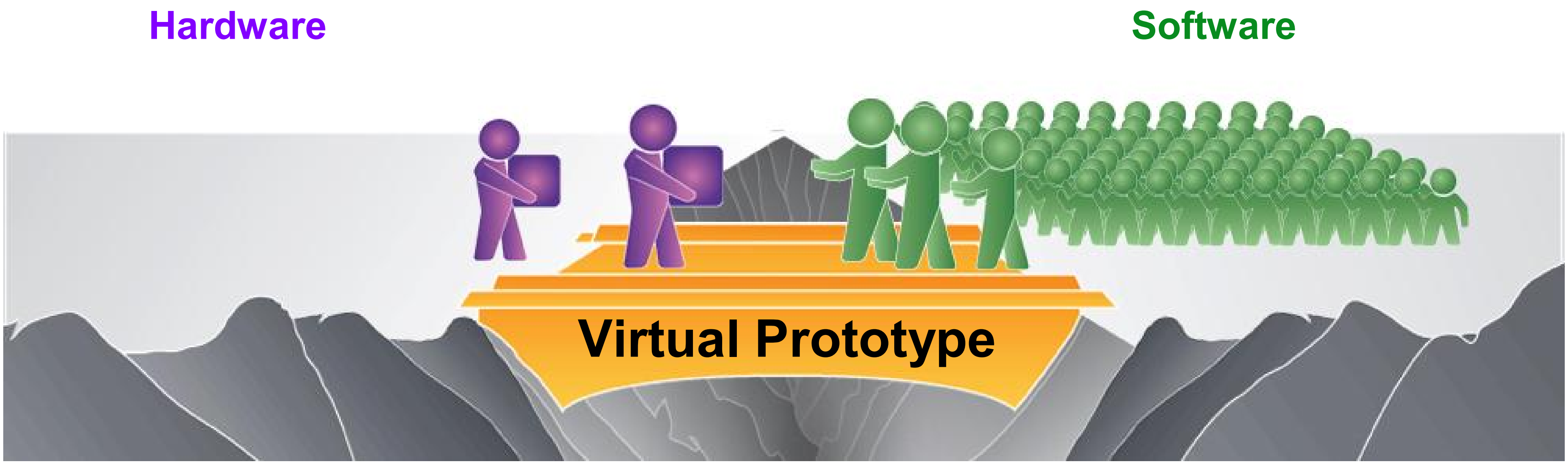
Hardware vs. Software



An Evolution of the "Traditional" Flow



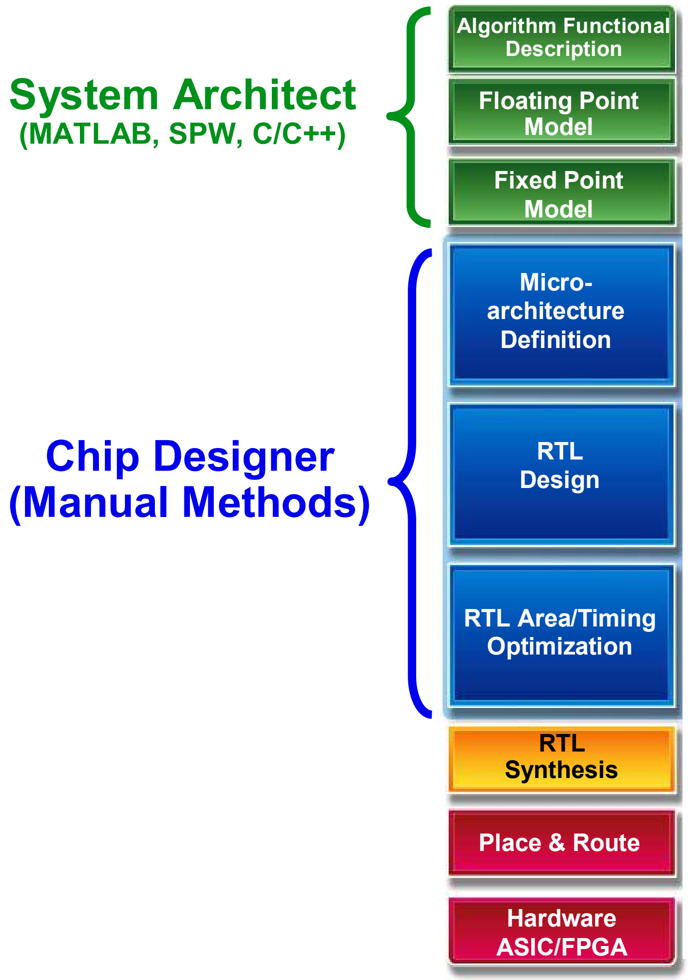
Hardware vs. Software



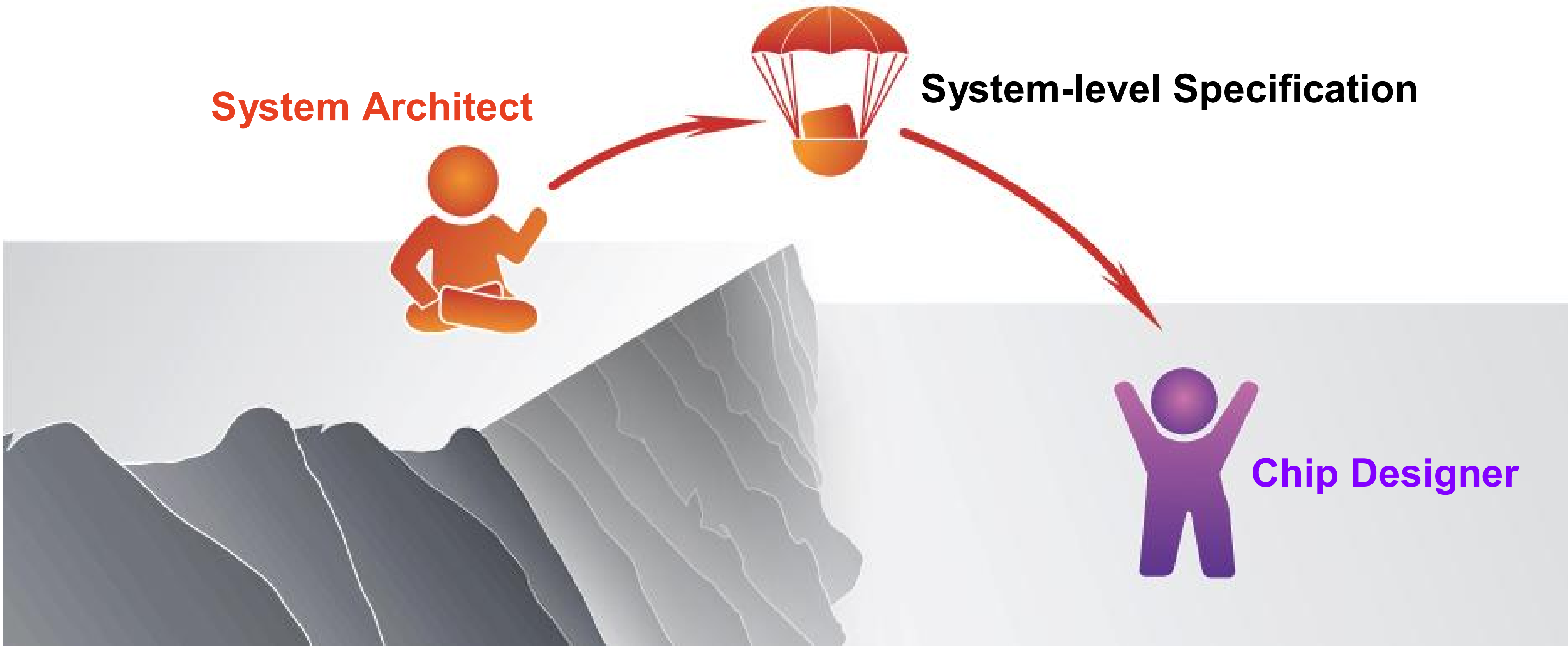
Sociology of Specialized Product Development Functions

- Hardware vs. Software
- System Architect vs. Chip Designer

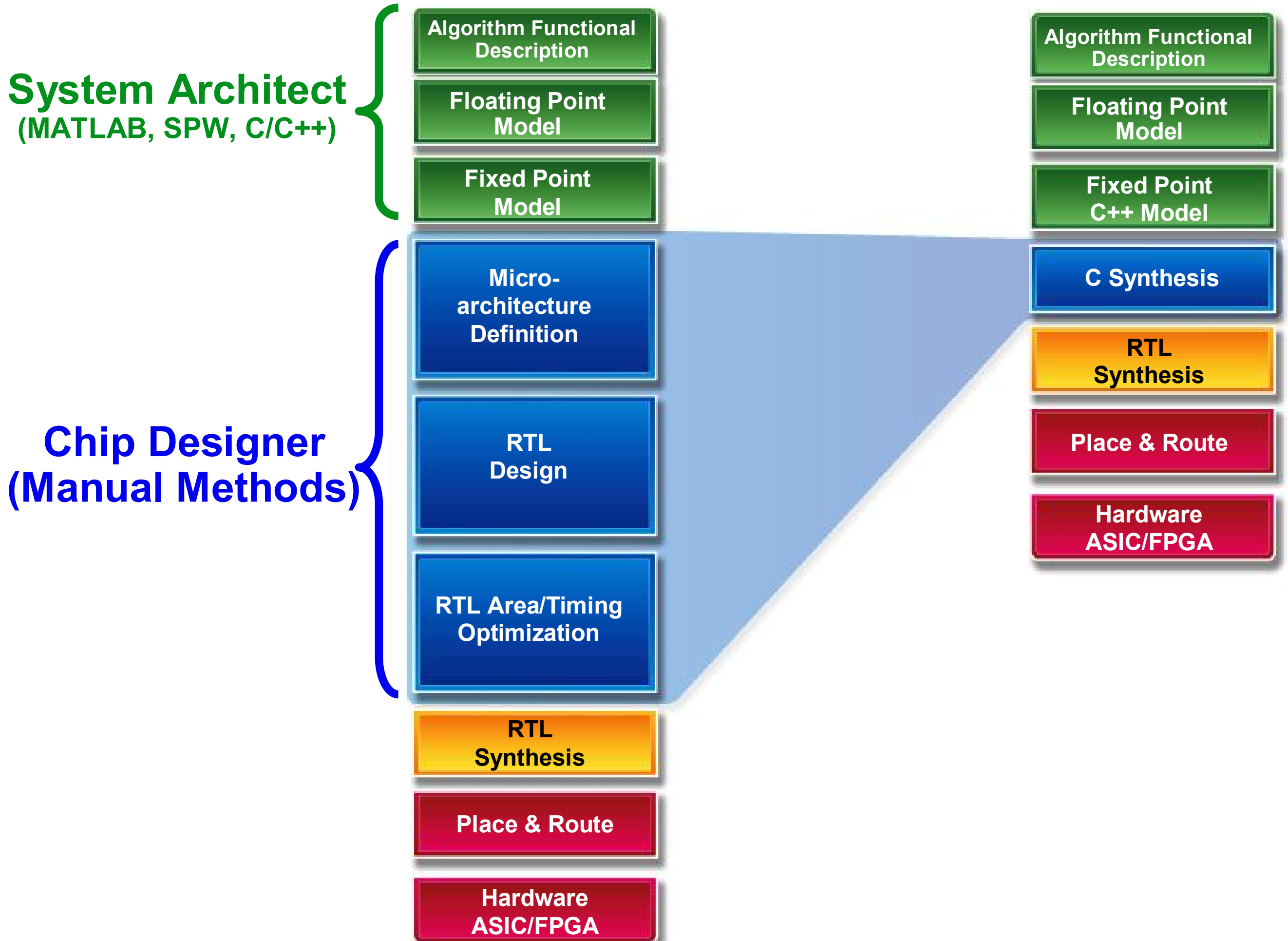
Manual Methods Slow Hardware Development



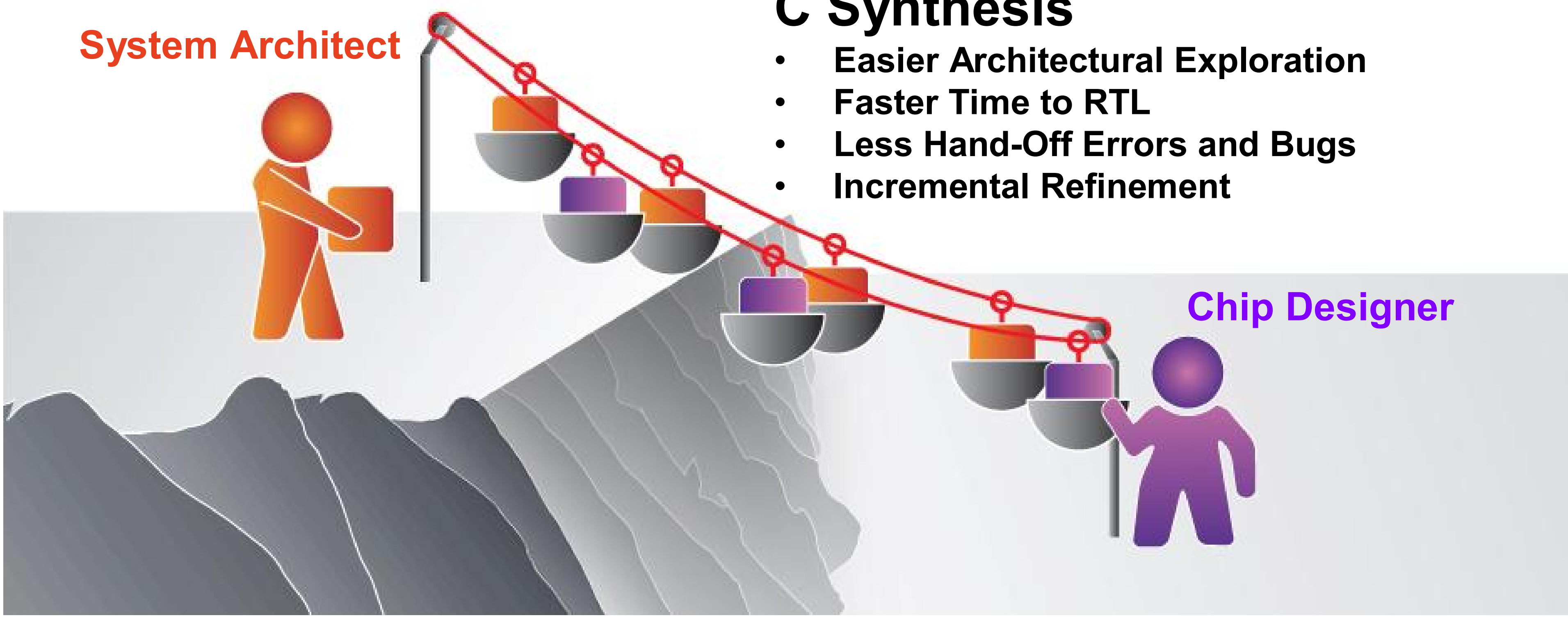
System Architect vs. Chip Designer



C Synthesis Enables Faster Architectural Exploration and Shorter Time to RTL



System Architect and Chip Designer



C Synthesis

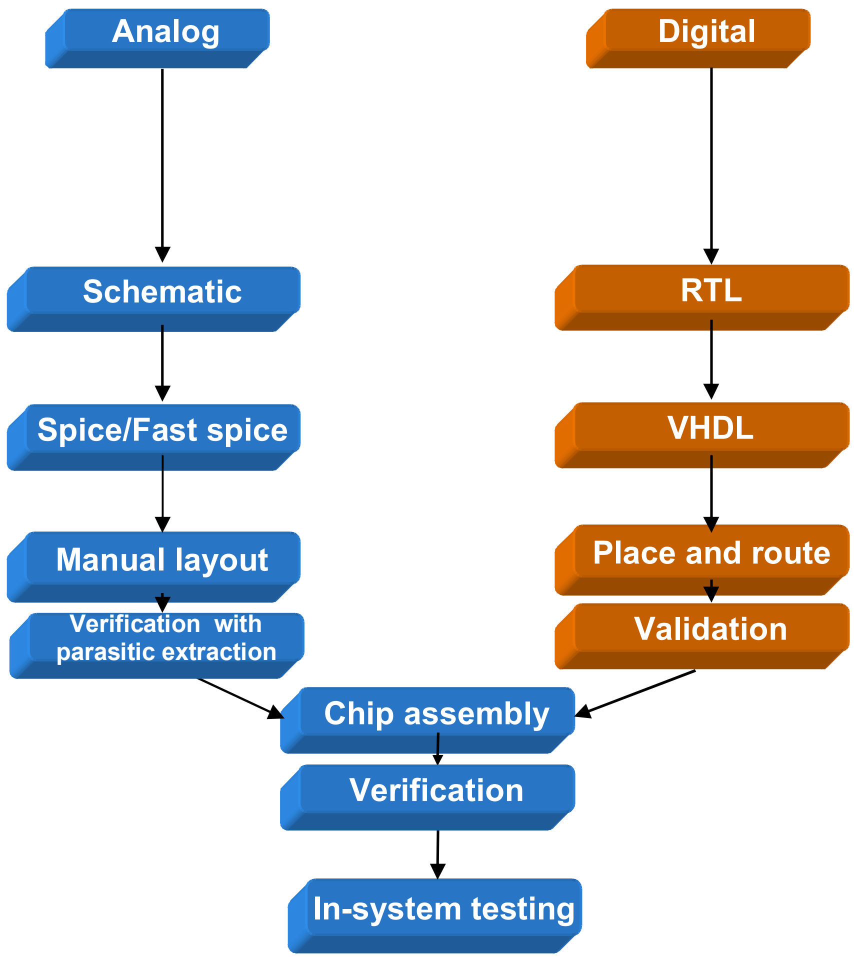
- Easier Architectural Exploration
- Faster Time to RTL
- Less Hand-Off Errors and Bugs
- Incremental Refinement

Sociology of Specialized Product Development Functions

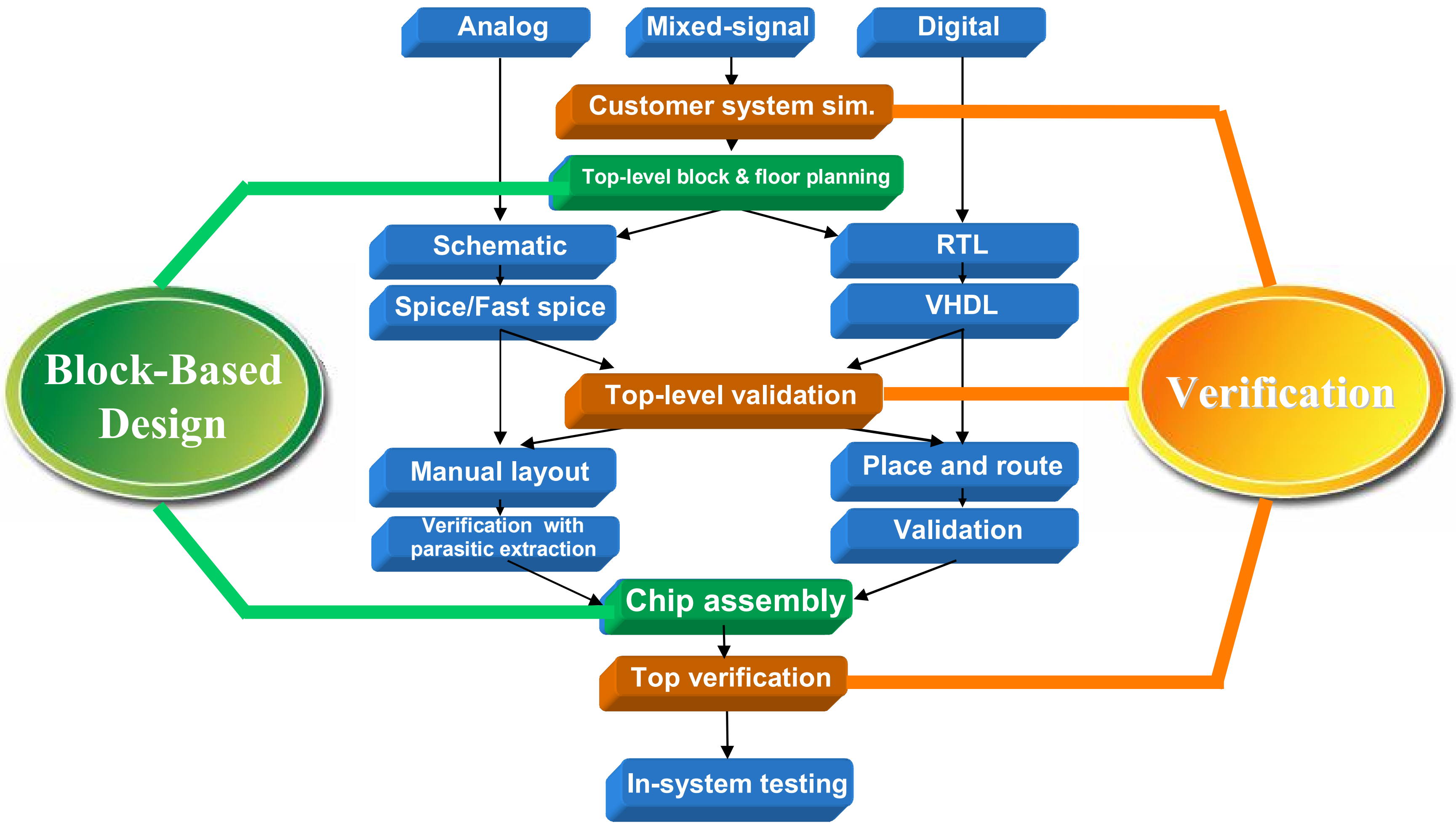
- Hardware vs. Software
- System Architect vs. Chip Designer
- **Digital vs. Analog**

Analog Design vs. Digital Design

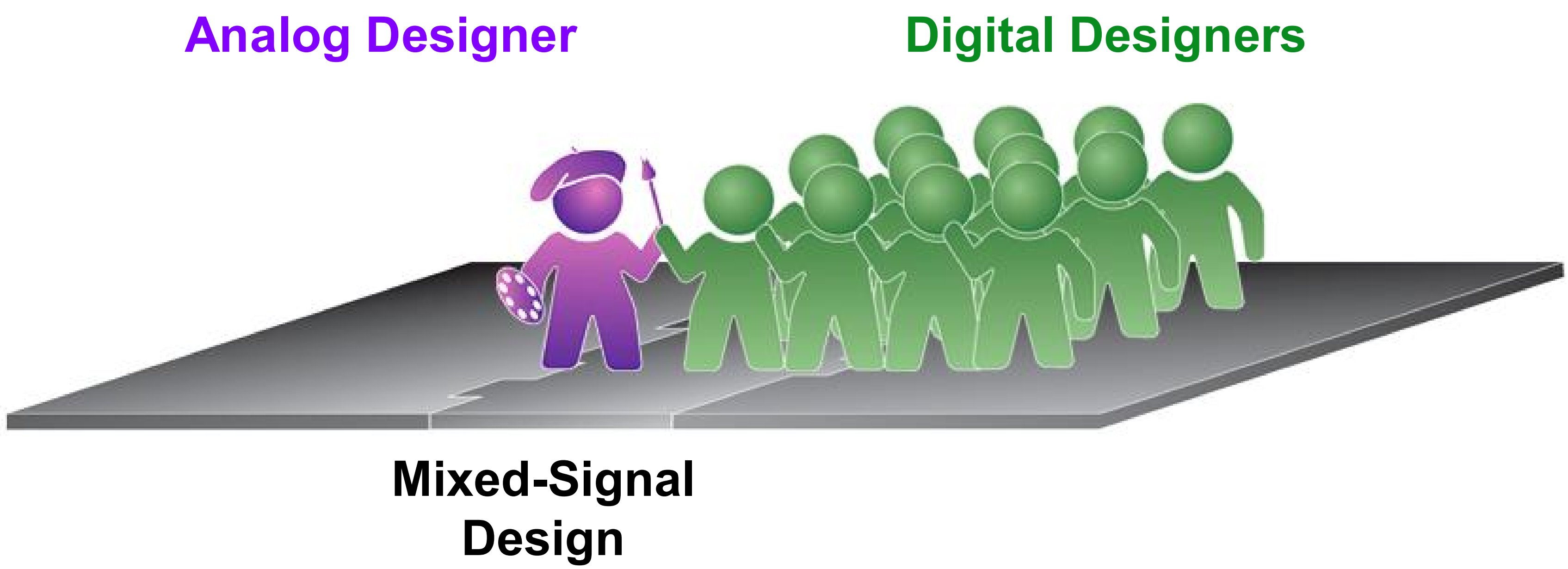
Today’s Analog and Digital Design Flows



Evolution of True Mixed-Signal Design Flows



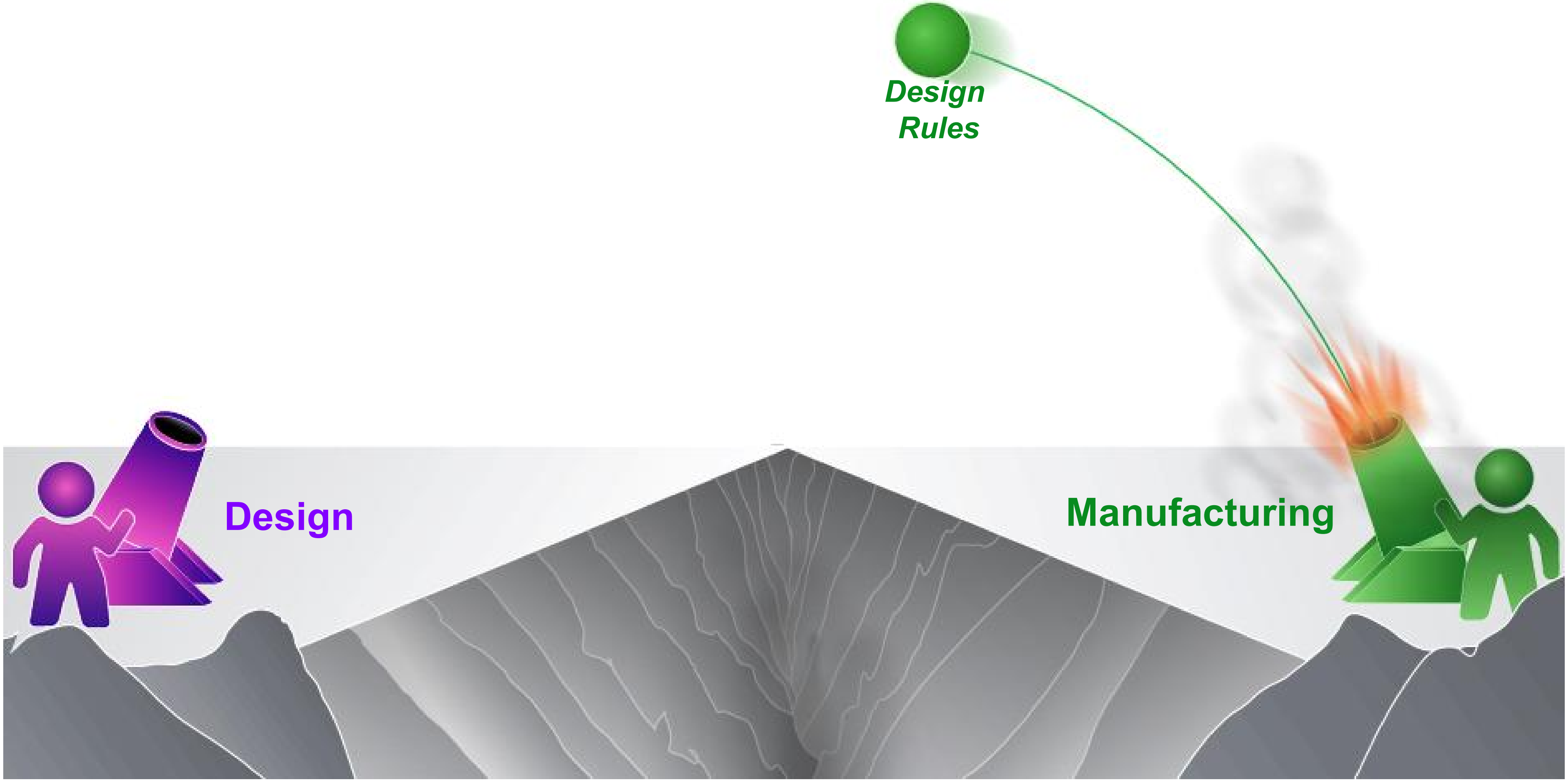
Analog Design and Digital Design



Sociology of Specialized Product Development Functions

- Hardware vs. Software
- System Architect vs. Chip Designer
- Digital vs. Analog
- **Design vs. Manufacturing**

Traditional Cooperation Between Design and Manufacturing



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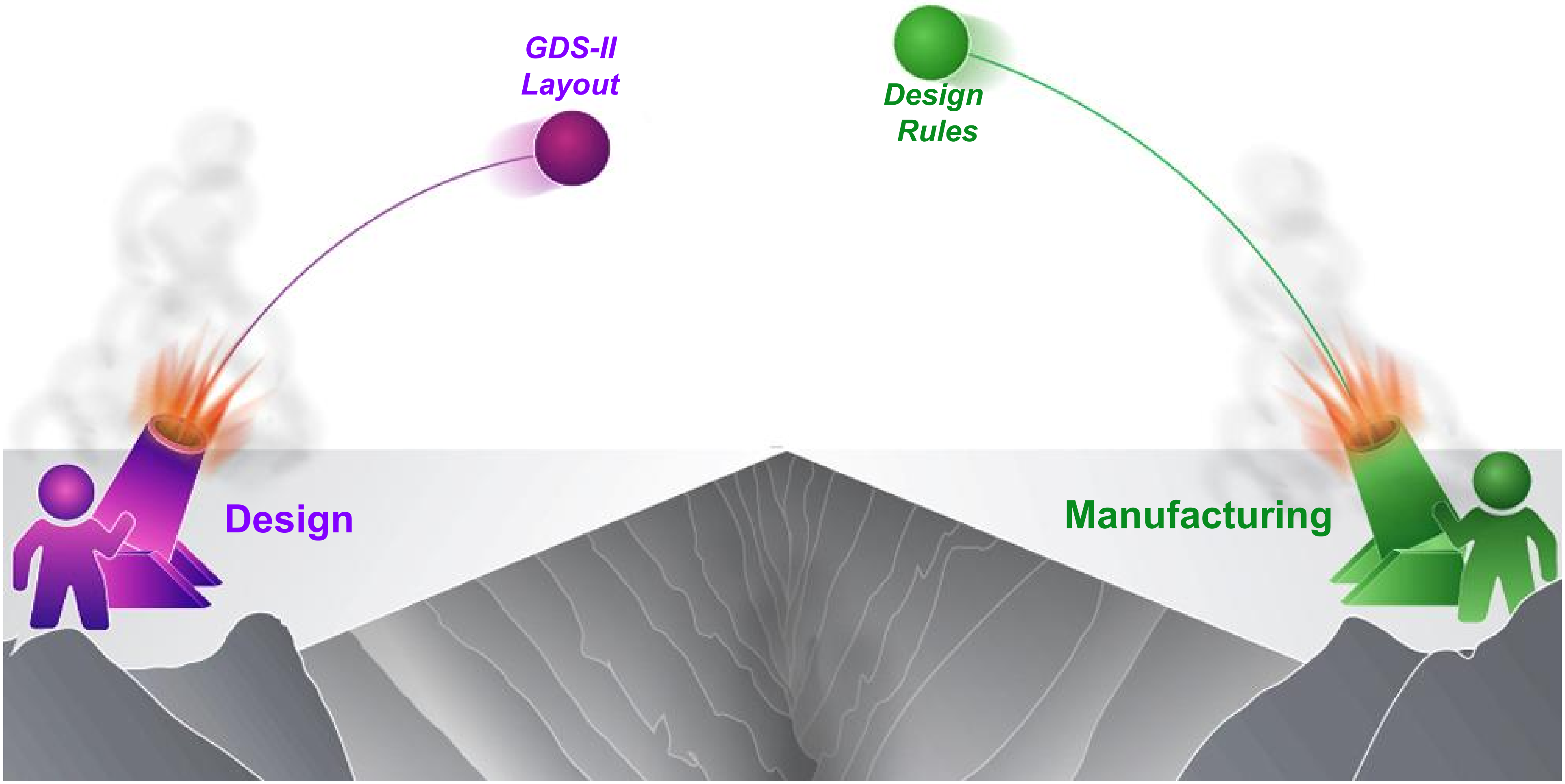
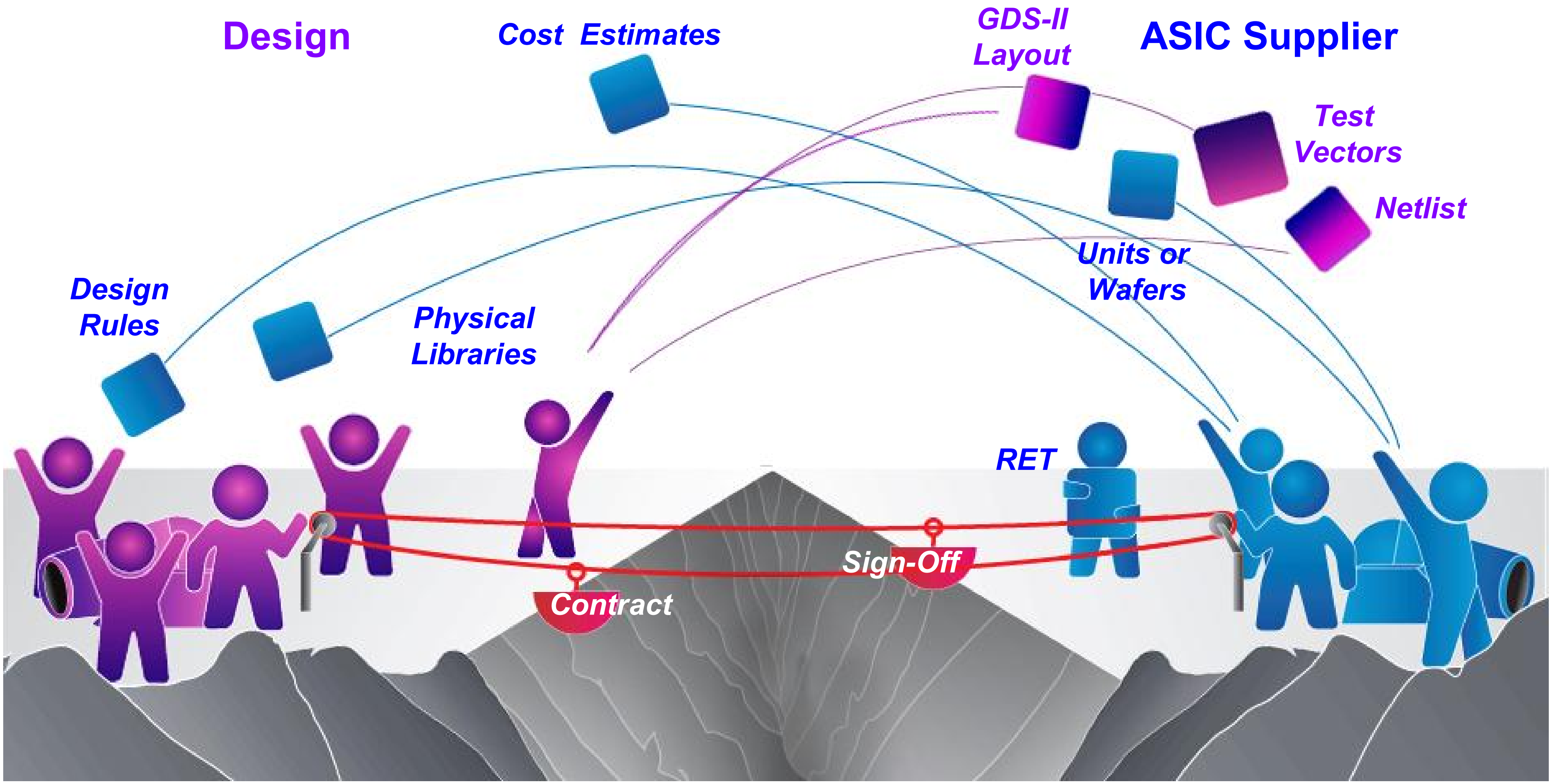
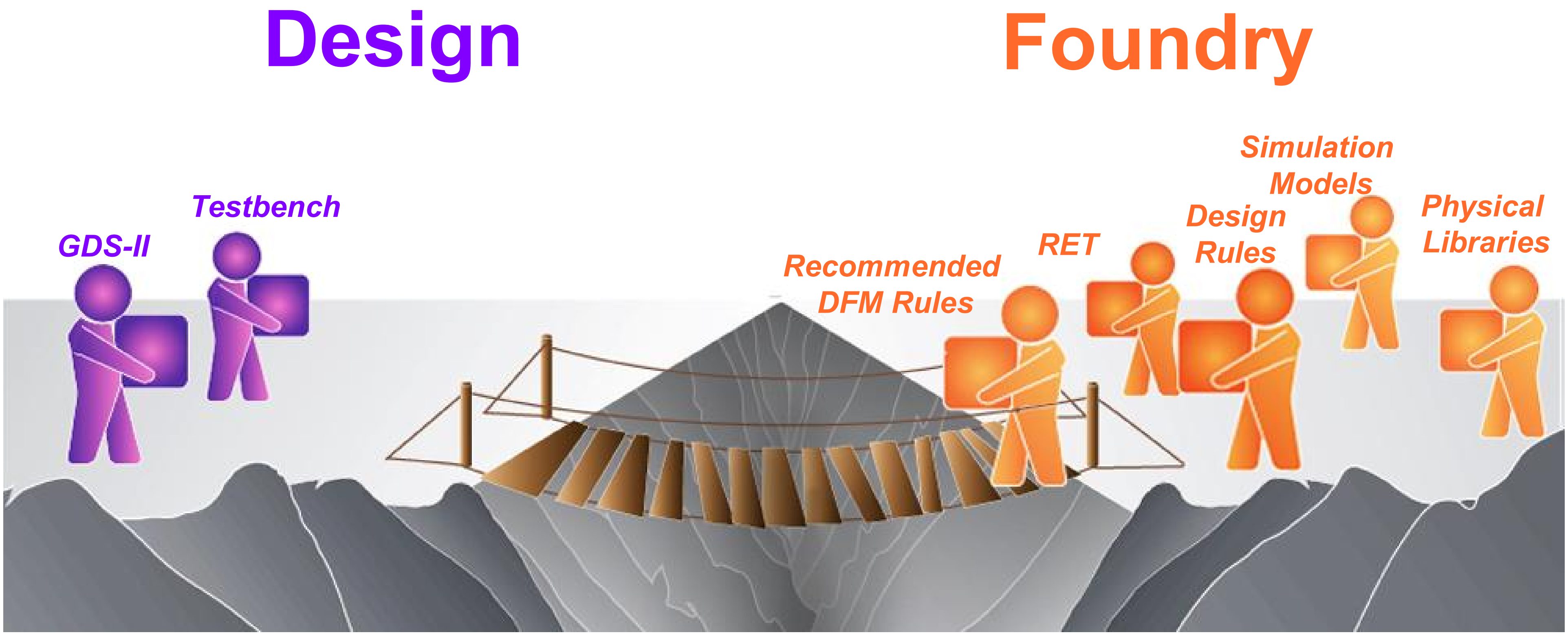


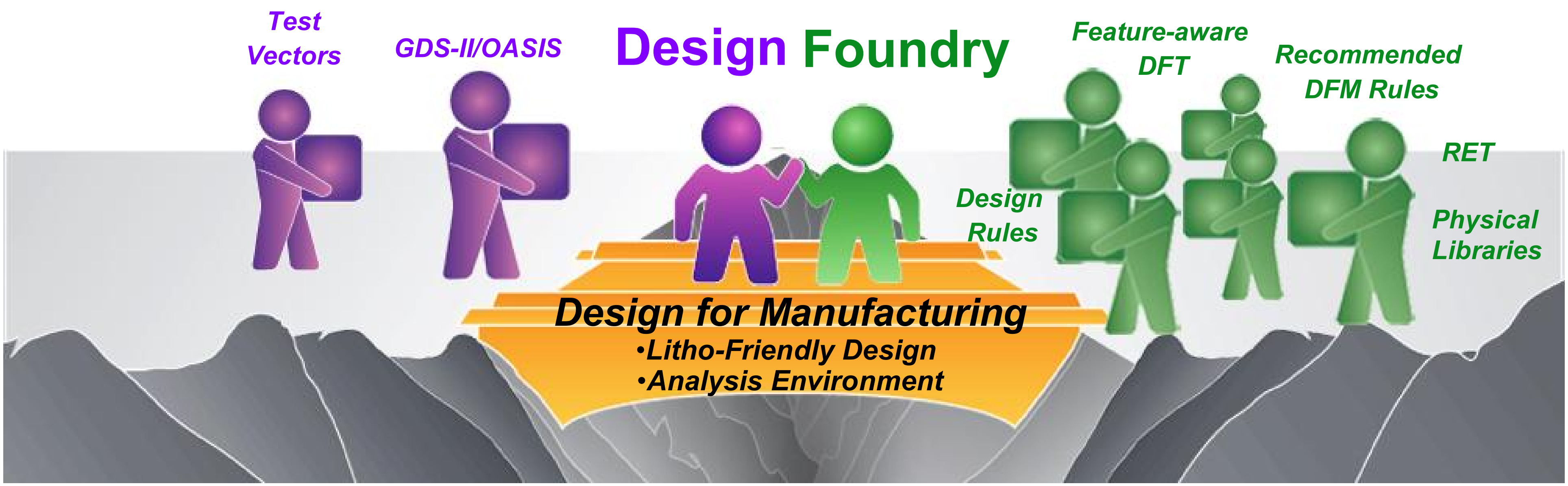
ASIC Requires Formalized Design/Manufacturing Information Exchange



Further Information Exchange With the Foundry Model

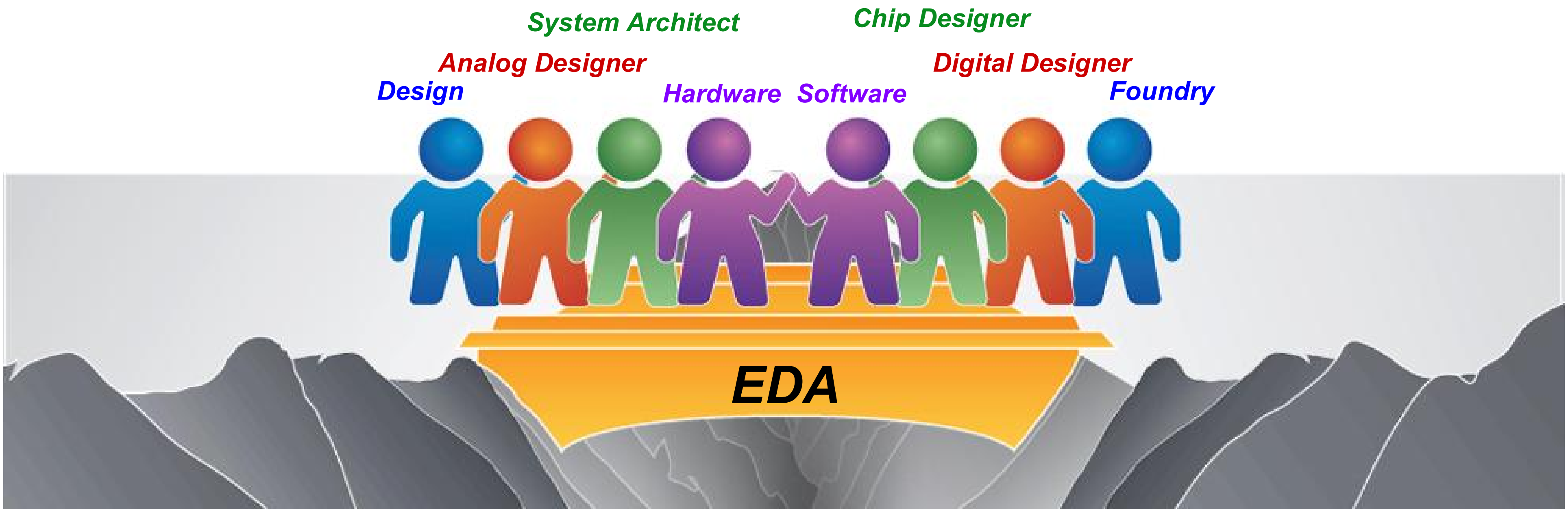


DFM Bridges Design and Manufacturing



EDA Provides the Bridge

- *Hardware/Software Virtual Prototype*
- *Synthesis from C++ to RTL*
- *Analog/Mixed-Signal Design*
- *Design for Manufacturing*



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