ModelSim™ designer

Increased Productivity From Creation to Realization

Darron May
Product Marketing Manager
Design, Verification &
Test Division

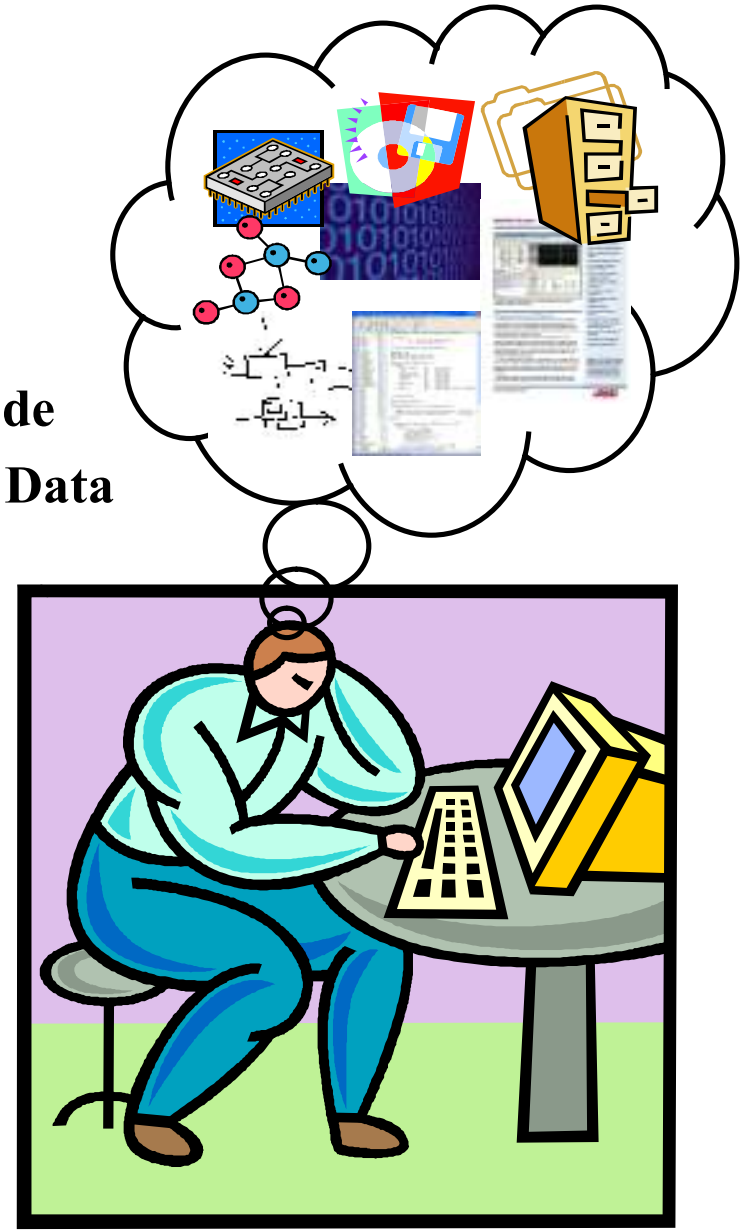
Mentor Graphics®

Agenda

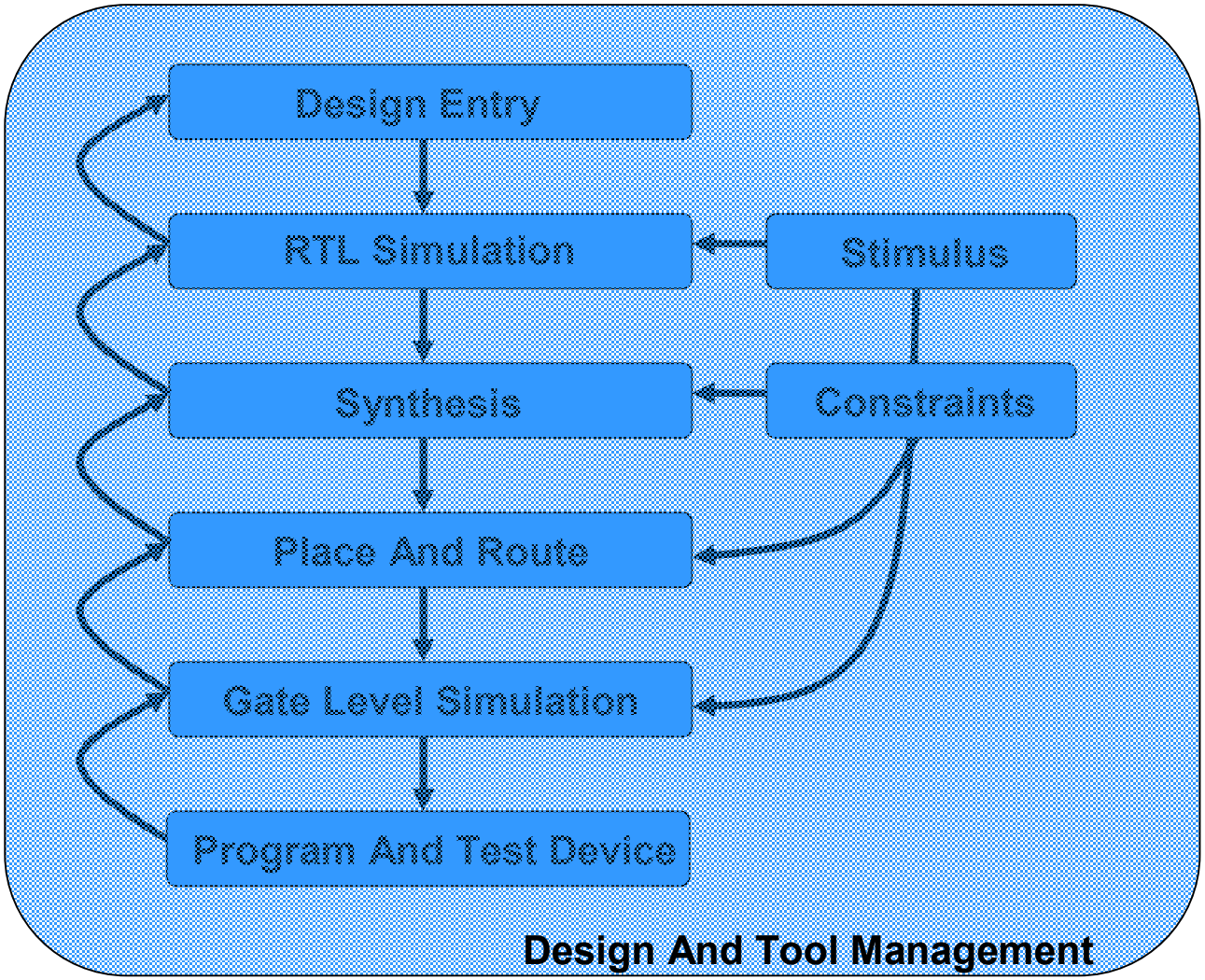
- Introduction
  - FPGA Design Flows
  - Vendor Tools
- ModelSim Designer
  - Features
  - Packaging
  - Options
- Product Demonstration

FPGA Design Evolving

- **Designs Are Getting Larger**
  - Larger Devices
  - HDL Design, Having To Write More Code
  - Having To Keep Track Of More Design Data
- **Designs Are Getting More Complex**
  - Having To Re-use Old Design Blocks
  - Having To Use 3rd Party IP
- **Design Flow Needs Management**
  - More Steps Required To Implement
  - Having To Manage The Design Tools
- **Market Windows Shrinking**
  - Need To Complete Designs Faster

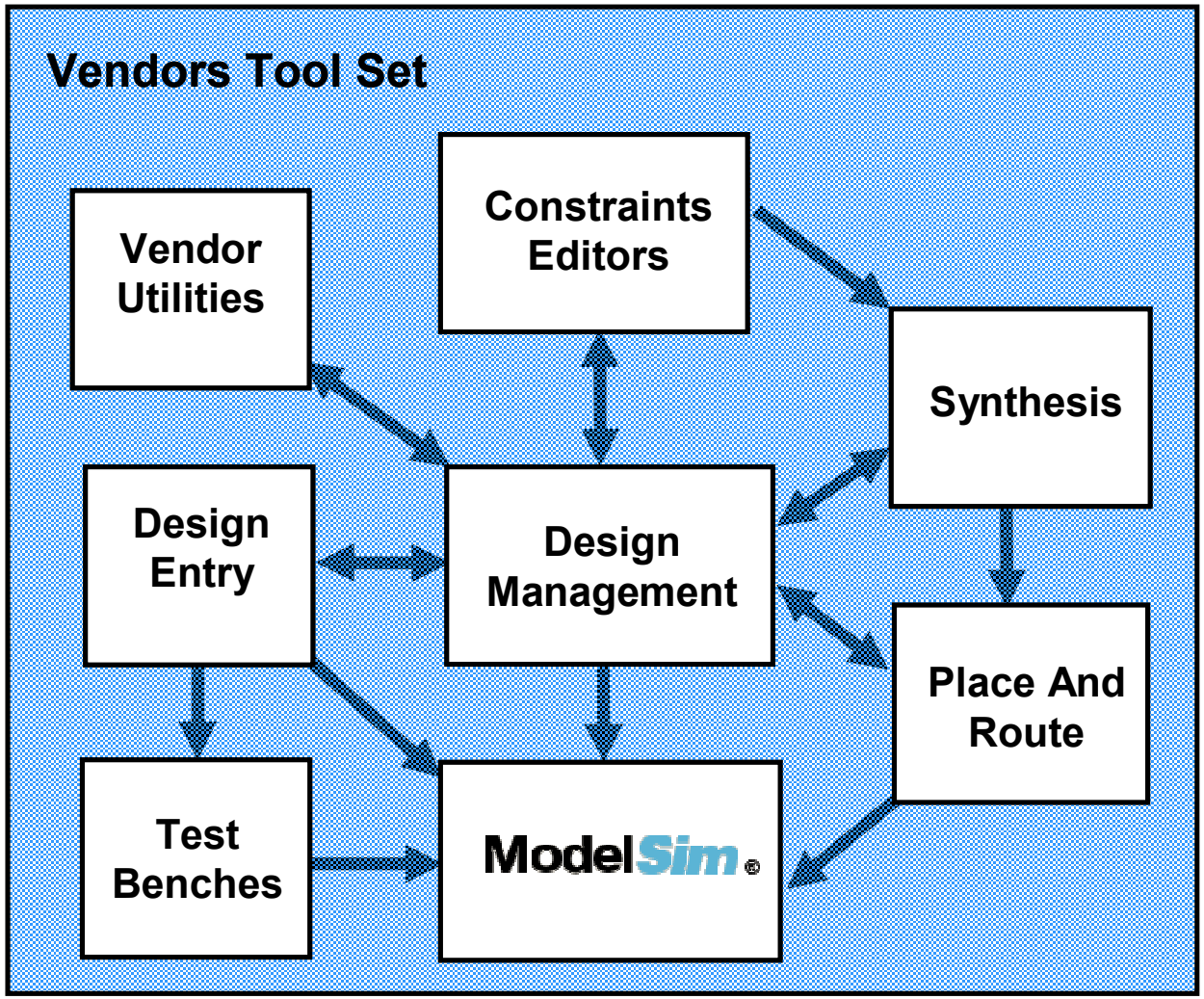


Typical HDL FPGA Design Flow



- Design Entry
  - HDL Editor
  - Graphical Editors
  - IP Use
  - Core Generators
- RTL Simulation
  - Test Benches
  - Functional Debug
- Synthesis
  - Text Constraints
  - Vendor Editors
- Place And Route
  - Text Constraints
  - Vendor Editors
- Gate Level
  - Re-use Stimulus
  - Optional Step
  - Library Compile
  - Netlist & SDF Files
- Program And Test
  - Debug
- Management
  - Design Data
  - Tool

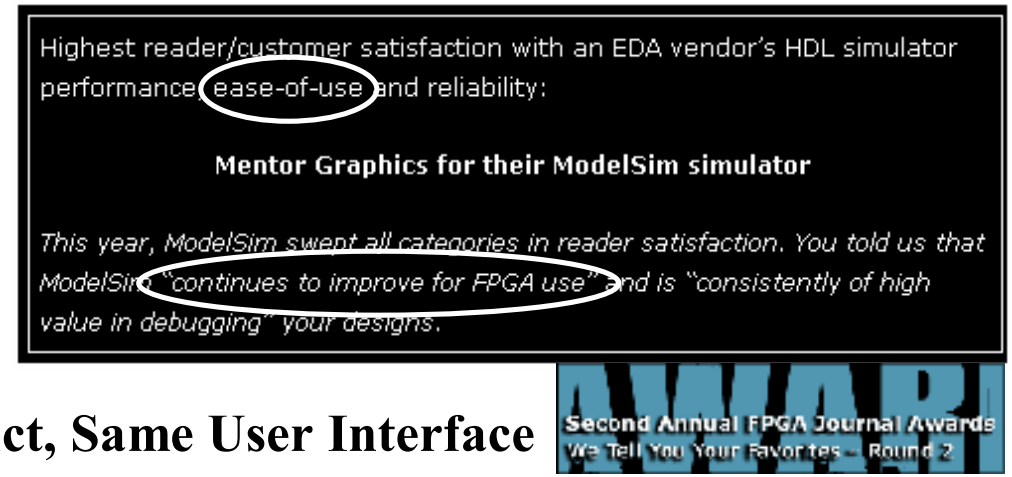
Current Vendor Tool Sets



- Vendors Tools
  - Actel Libero
  - Altera Quartus
  - Lattice ispLEVEL
  - Xilinx ISE
- Design Entry
  - Limitations
  - Not A Focus
  - Not Complete
- Simulation
  - Integration With MS
  - OEM Versions
- Synthesis
  - Altera QIS
  - Leonardo
  - Precision
  - Synplify
  - Xilinx XST
- Place And Route
  - Own Tools
  - Chip Level Utilities
- Management
  - Limited
  - Vendor Specific

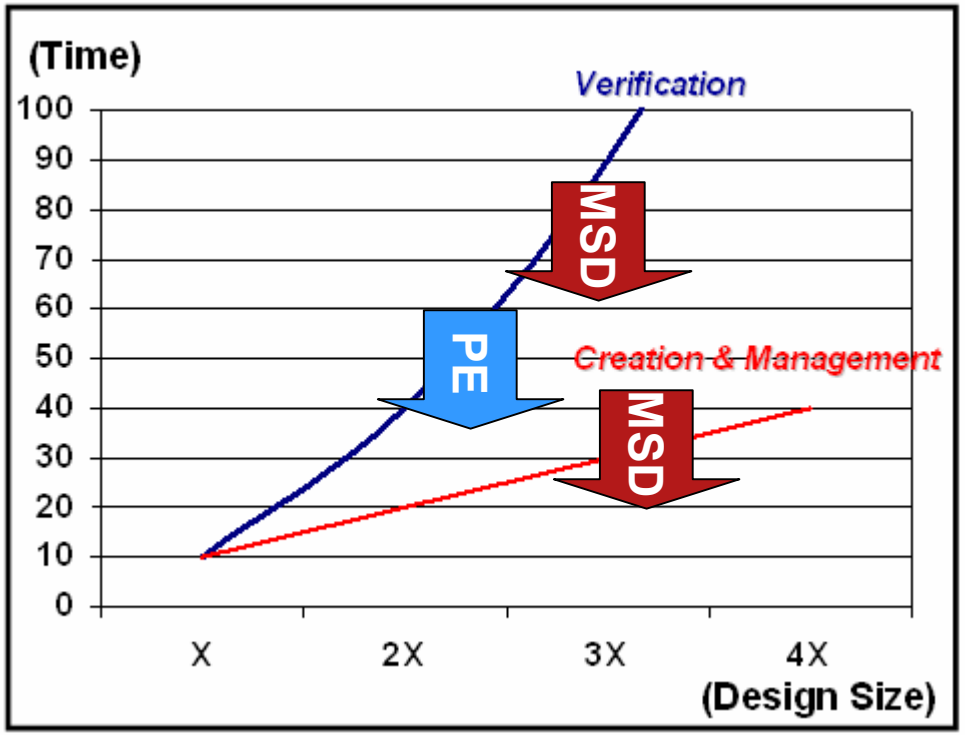
ModelSim OEM Product

- **ModelSim OEM Versions**
  - **ModelSim XE III (Xilinx)**
  - **ModelSim AE (Altera)**
  - **ModelSim Actel Edition**
  - **ModelSim Lattice Edition**
- **ModelSim Personal Edition**
  - **The Base Of The OEM Product, Same User Interface**
  - **Plug-in Replacement In All Vendor Tool Sets**
- **Comparing Personal Edition To OEM's**
  - **Performance And Capacity (2.5X-3X Faster)**
  - **Supports Multiple Vendors**
  - **Supports Mixed VHDL and Verilog**
  - **Supports SWIFT Interface Simulating Special Cores**
  - **Code Coverage And Design Profiler**
  - **Waveform Compare And Extended Dataflow**



ModelSim Focused FPGA Solutions

- **Personal Edition (PE)**
  - A Simple Solution To Larger Designs
  - Targets Verification Performance
  - Same Interface As OEM
  - 2.5X-3X Faster Than OEM
- **ModelSim Designer**
  - Performance + Productivity
  - PE Performance
  - Increase Productivity
    - Shrink Design Time
    - Shrink Debug Time



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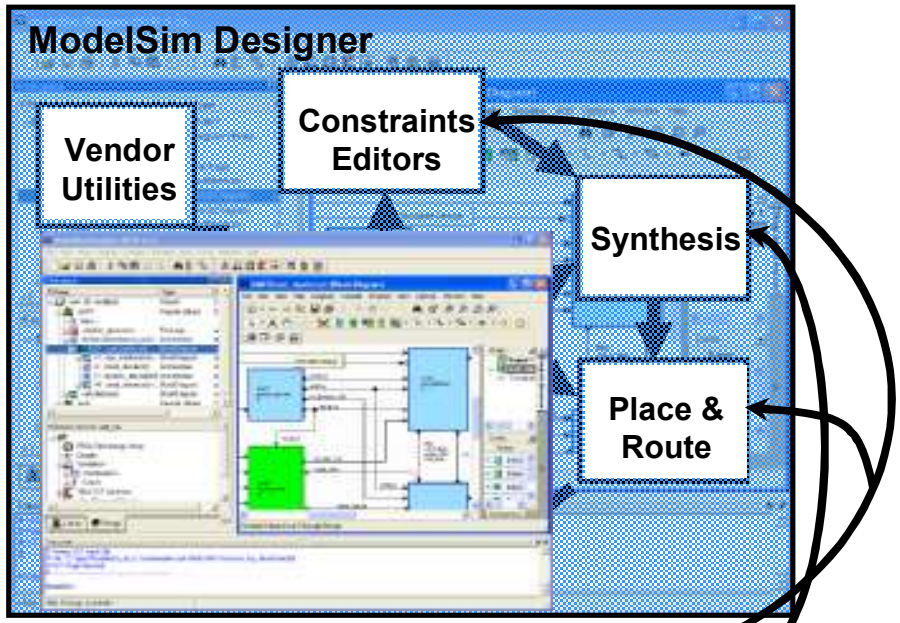
  - Vendor Tools
- **ModelSim Designer**
  - **Features**
  - Packaging
  - Options
- Product Demonstration

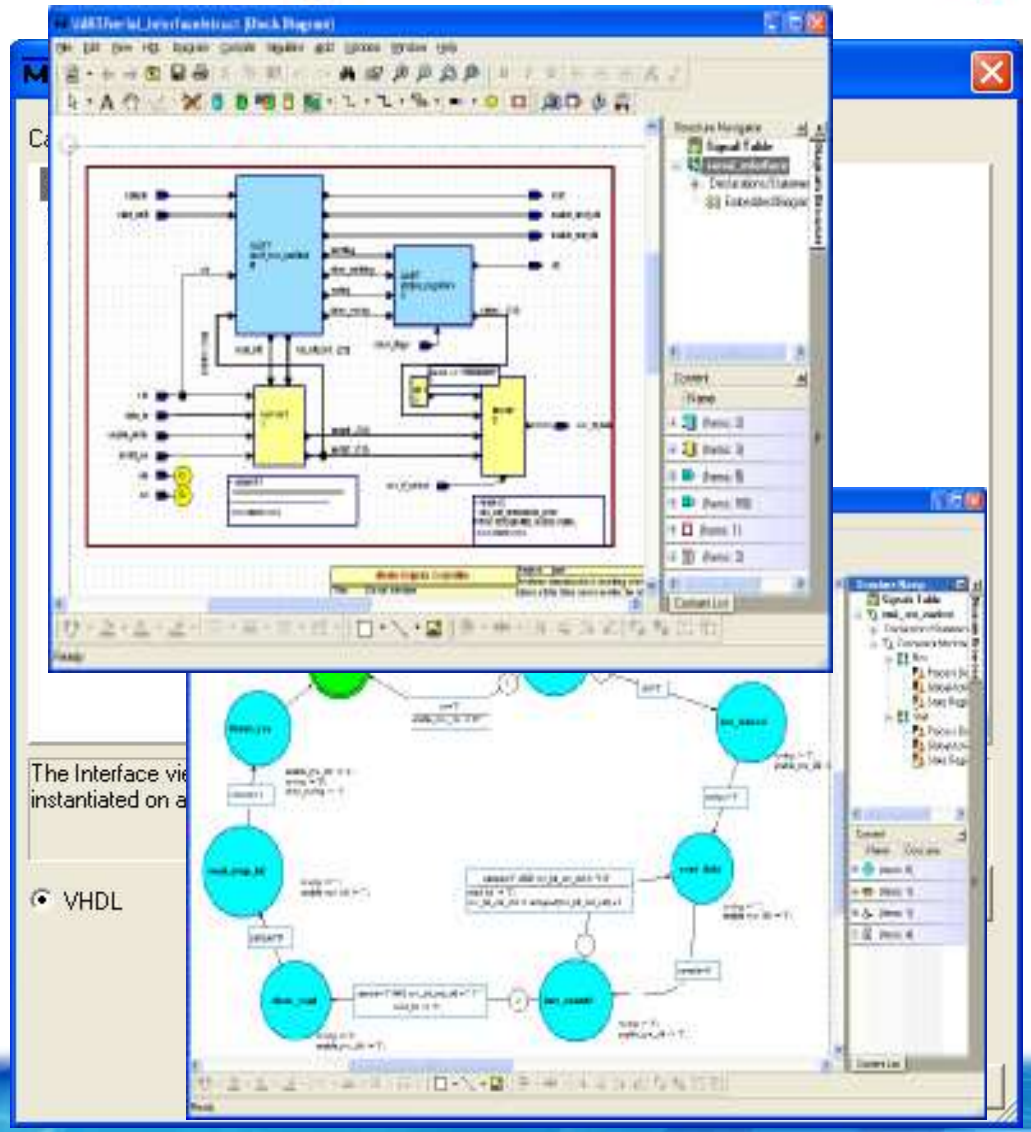
Creation To Realization

- **ModelSim Designer**
  - Manage Creation To Realization
  - Simple Easy To Use GUI
  - Based On Proven Technology
- **Product Drivers**
  - Great Value For Money
  - Automation & Organization
  - Ease-of-use, Desktop Tool
- **Powerful Features**
  - Implementation Integration
  - Creation, IP Re-use
  - Simulation At All Levels Of Abstraction
  - Design Management
  - Tool Flow Management



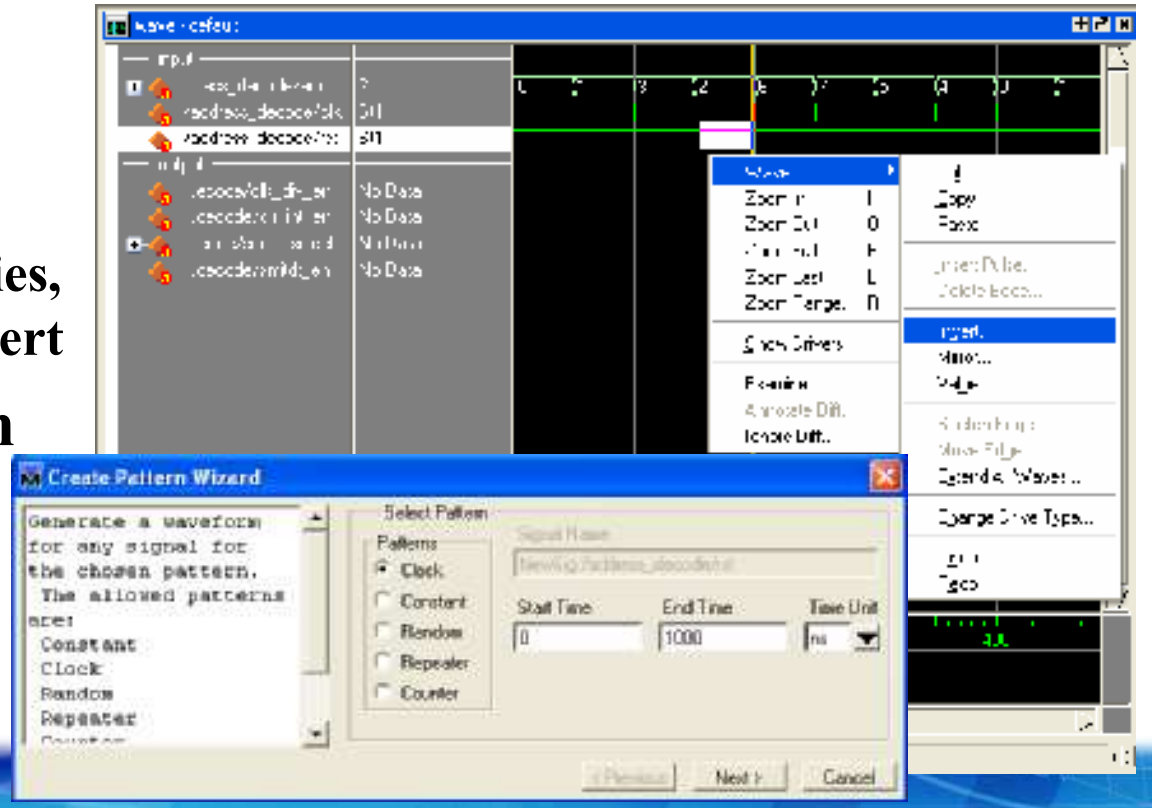
Faster Design Entry

- **Creation Wizard**
  - Ease Of Use
  - Choose Capture Method
- **Block Diagram Editor**
  - Create Design Structure
    - Bottom up, Top Down
- **State Diagram Editor**
  - Define Lower Level Detail
- **Benefits**
  - Self Documenting
  - Auto Generate HDL Code
  - Design Navigation & Understanding



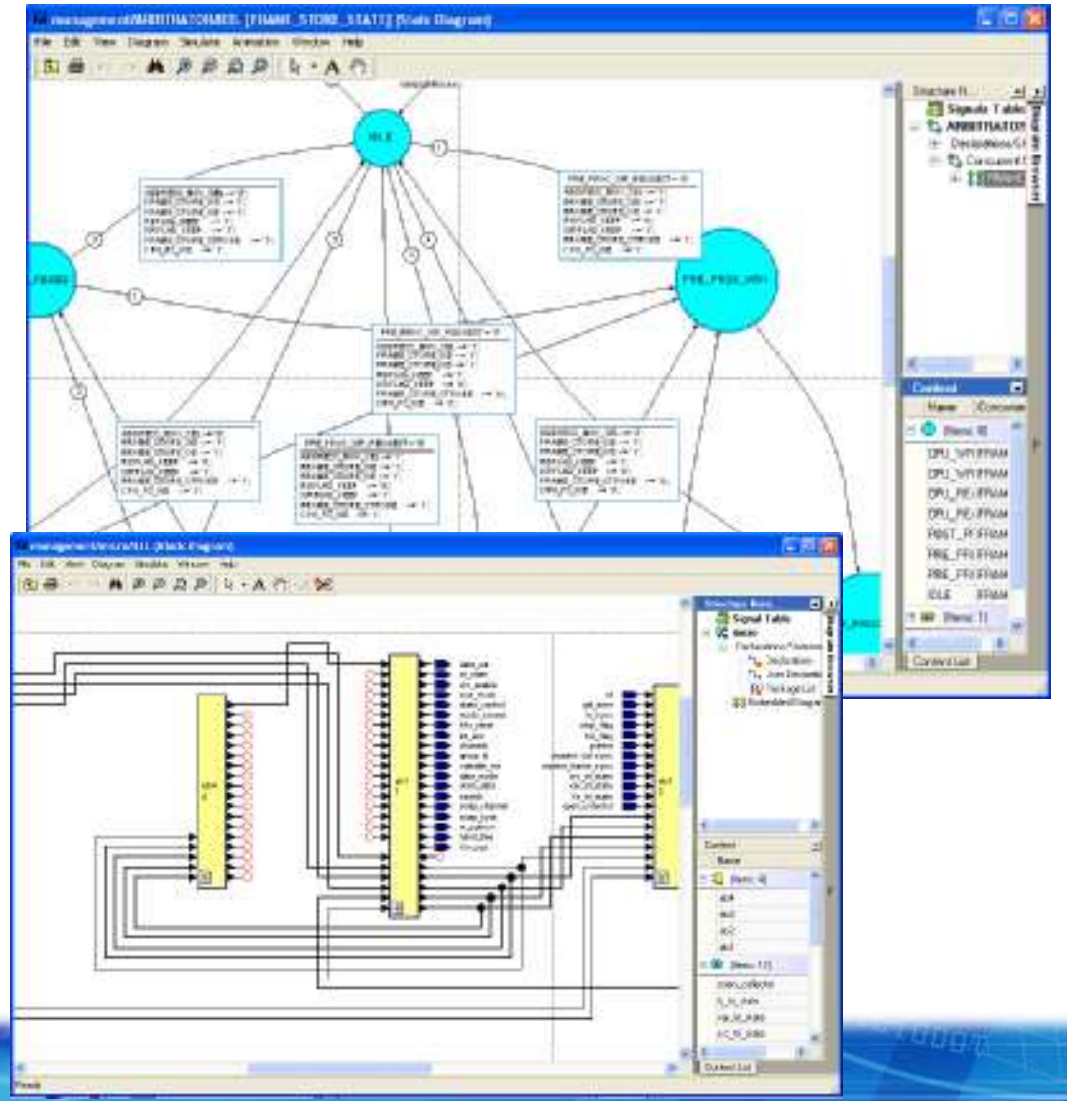
Faster Design Entry

- **Full Featured Text Editor**
  - Language Templates For Faster Text Entry
  - Cross Reference Between Graphics And Code
  - Quickly Track & Fix Errors During Compile & Simulation
- **Waveform Editor**
  - Fast Generation Of Stimulus Using Wizard
  - Flexible Edit Capabilities, Cut, Paste, Mirror, Invert
- **Test Bench Generation**
  - Harness Generation
  - Text Templates



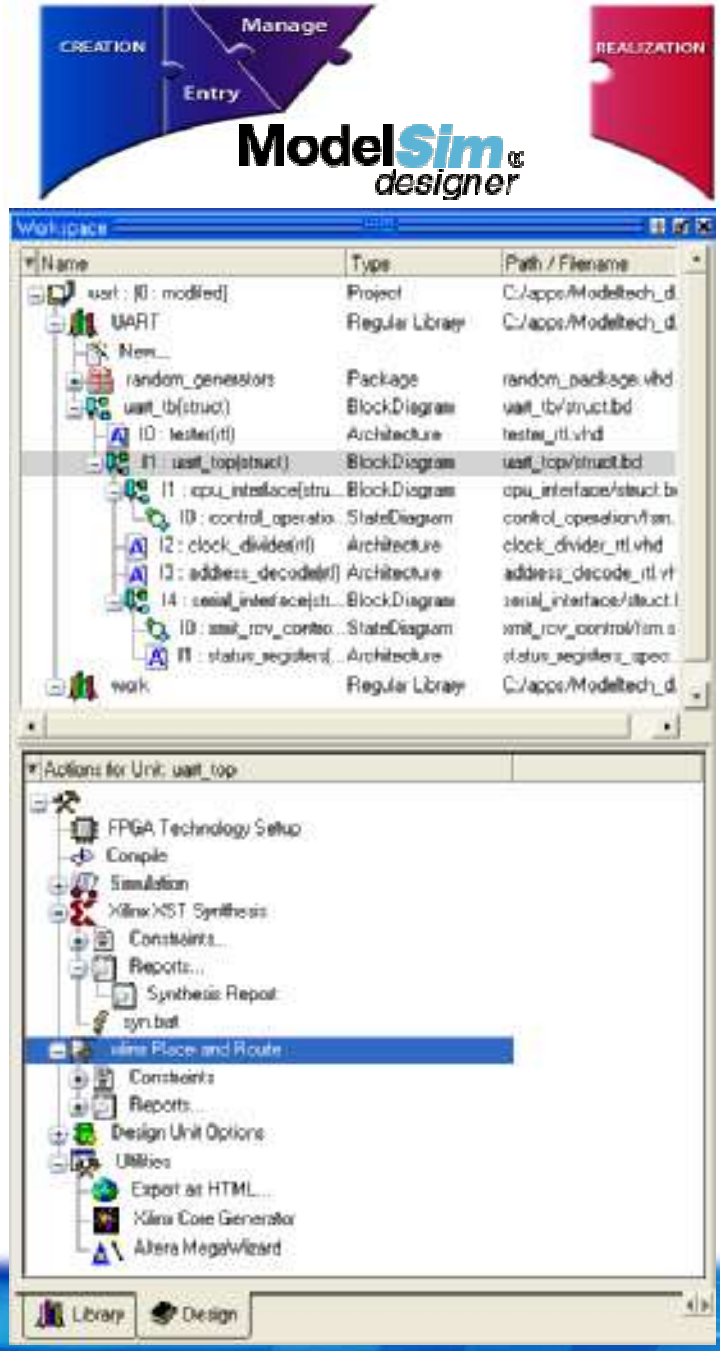
Design Comprehension

- **Import Existing IP**
  - Import Wizard
    - Re-use Any HDL Design
    - Re-use Sub Block
  - Import ModelSim Projects
  - Use ModelSim Do Scripts
- **Render Graphics**
  - Visualize HDL
    - Block Diagrams
    - State Diagrams
  - Simulate & Debug Graphics
  - Document Text Designs
  - Aids Communication



Design Management

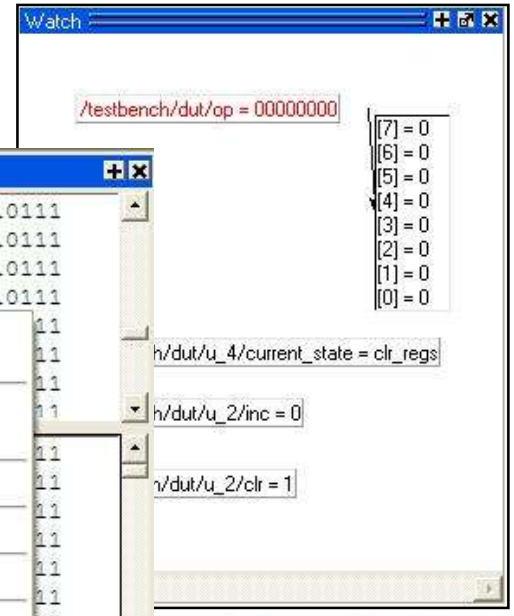
- **Projects & Libraries**
  - Flexible Design Organization
  - Hierarchical Design Navigation
  - Manage Design & Project Data From One Location.
- **Easy To Use Actions Pane**
  - Context Sensitivity Aids Tool Learning
  - Organize Design And Tool Data
  - Manage Scripts And Constraints
  - View All Tool Report Files
- **Project Archiving**
  - Version Control Management
  - Manage All Tools Data
  - Quickly Retrieve Design Changes



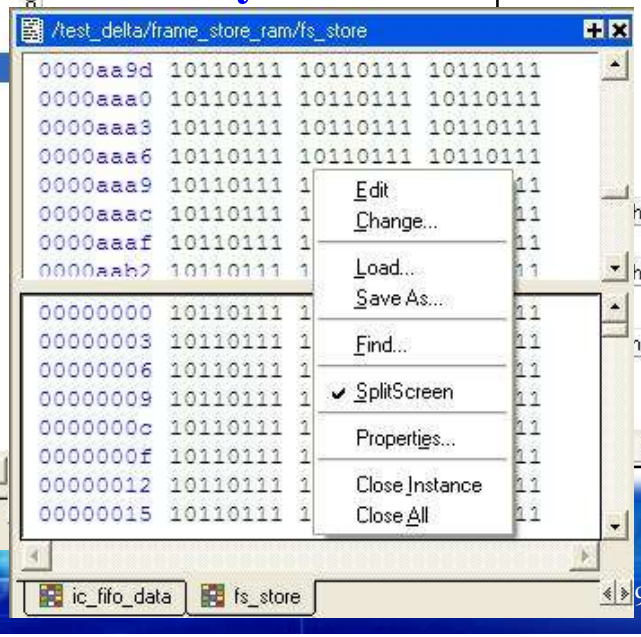
Simulation & Debug

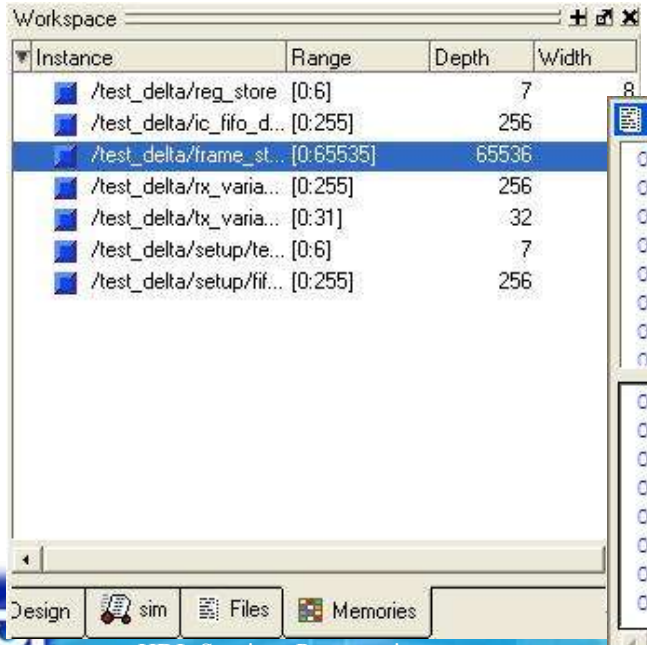
- **ModelSim Simulation And Debug**
  - **Proven & Powerful Source Level Debugging Environment**
    - **Break points, single step, waveform viewer**
  - **Mixed VHDL & Verilog**
  - **Multiple Connected Simulation Data Views**
    - **wave, structure, source, objects, dataflow**

Watch



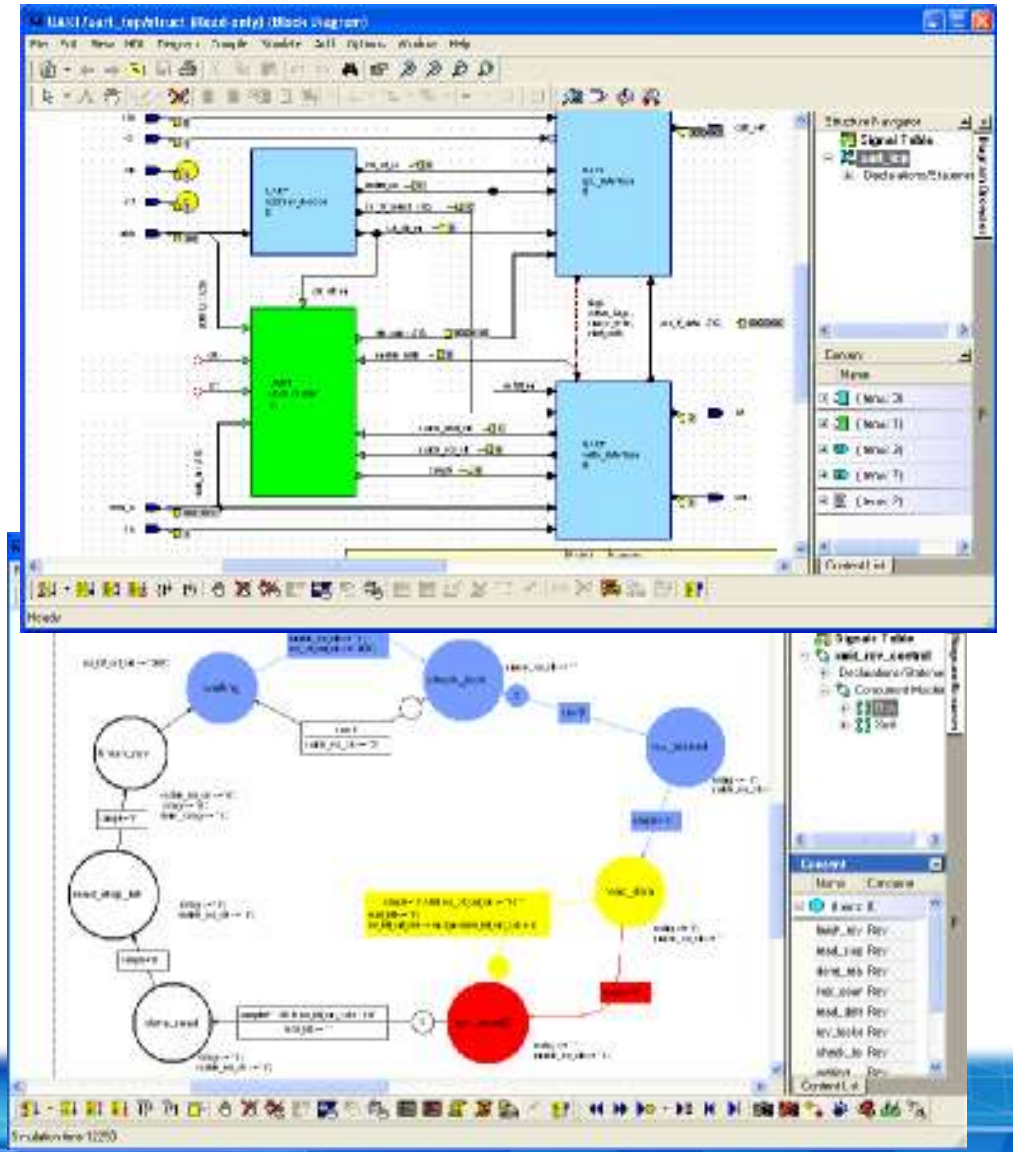
Memory



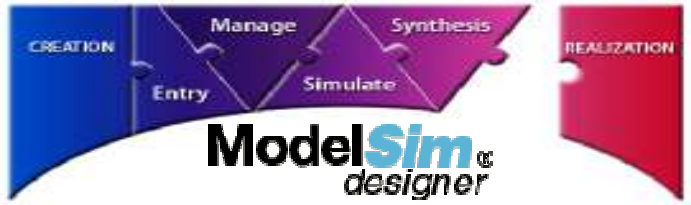


Simulation & Debug

- **Debug With Graphics**
  - Set Breakpoints And Probes On Block Diagrams
  - Powerful State Machine Animate & Playback
  - Linked To Source
- **Script Management**
- **Automation Of Post P&R Simulation Steps**
  - FPGA Library Compiler
  - Netlist Management
  - Automatic SDF Annotation
- **OEM Aware Mode**



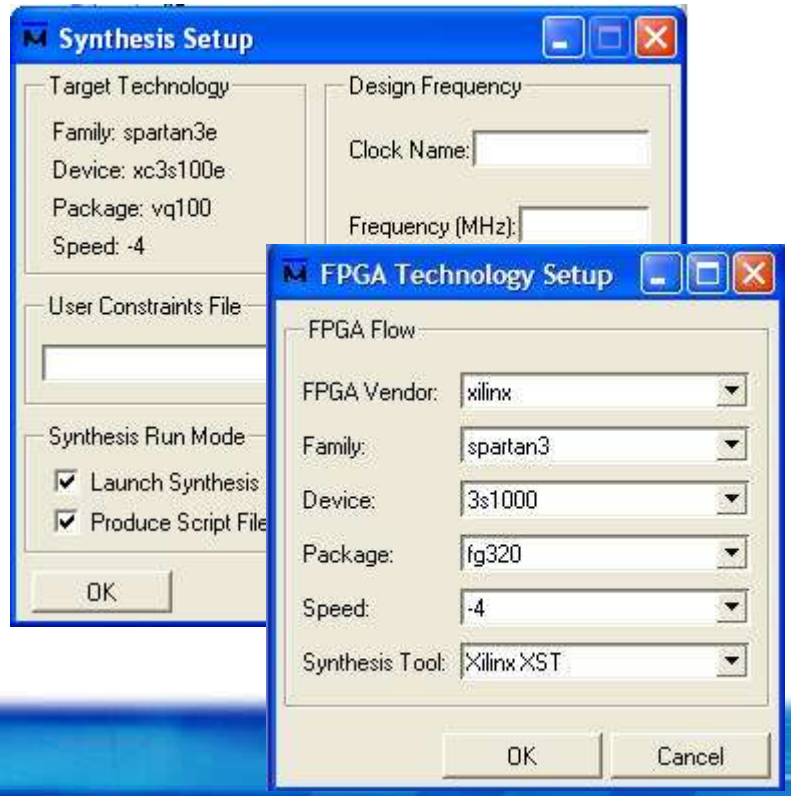
Synthesis



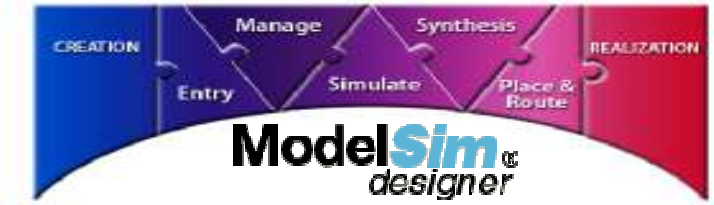
- **Integrates With Most Popular Synthesis Tools**
  - XST, QIS, Leonardo Spectrum, Precision, Synplify, Synplify Pro

ALTERA. XILINX® Mentor Graphics® Synplicity®

- **Automatic Setup**
  - Tool Detection & Options Section
  - Flow Repeatability
- **Flexible Execution**
  - Run And View Results In Single GUI
  - Output Scripts To Run Externally
- **Complete Management Of Process**
  - Edit And Attach Constraint Files
  - View Report Files



Place & Route



- Integrates With Most Popular P&R Tools
- Automatic Setup
  - Detection & Options Section
  - Flow Repeatability
  - Vendor Independence
- Flexible Execution
  - Run And View Results In Single GUI
  - Output Scripts To Run Externally
- Automatic Data Management
  - Gate Level Netlist & Libraries
  - SDF & Instance Annotation
  - Vendor Constraint Tool Usage
  - Consistence Data Management

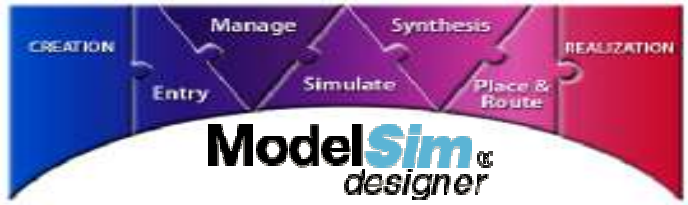
Actel

ALTERA

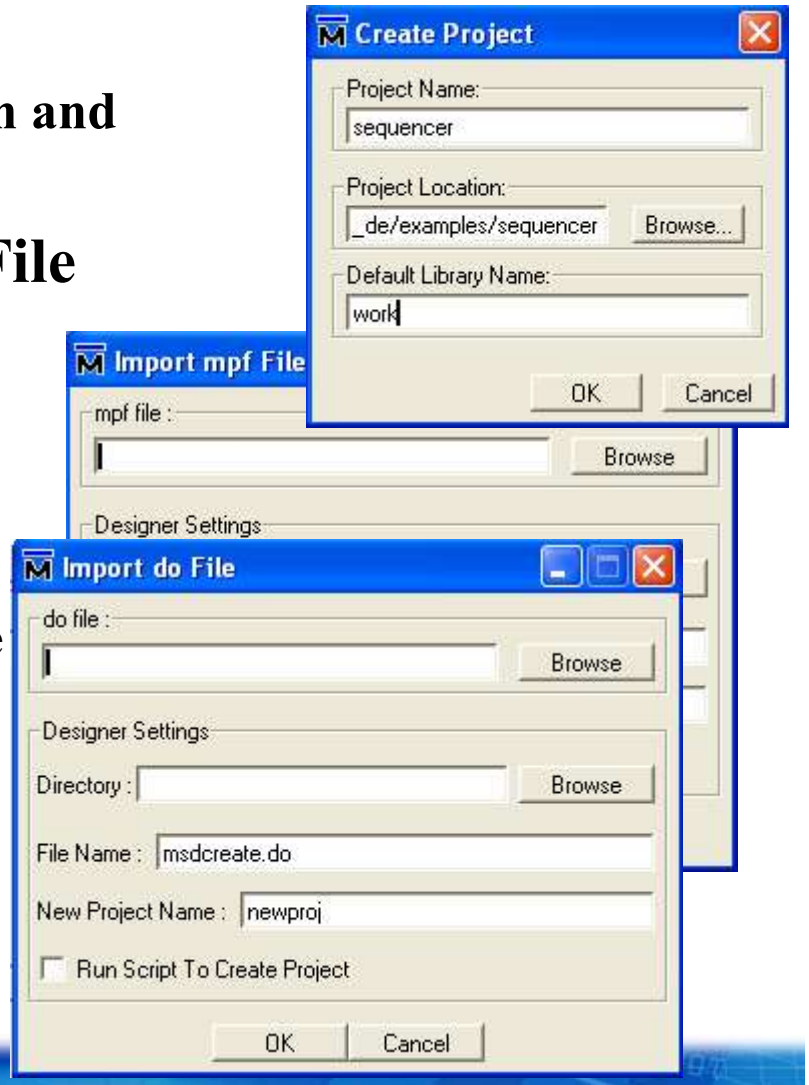
Lattice Semiconductor Corporation

XILINX

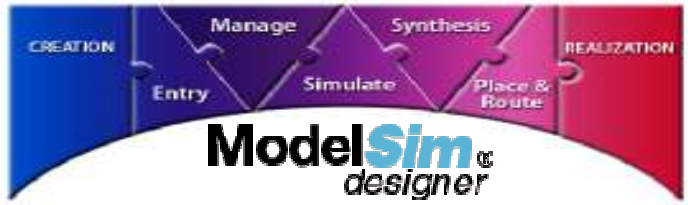
Using ModelSim Designer



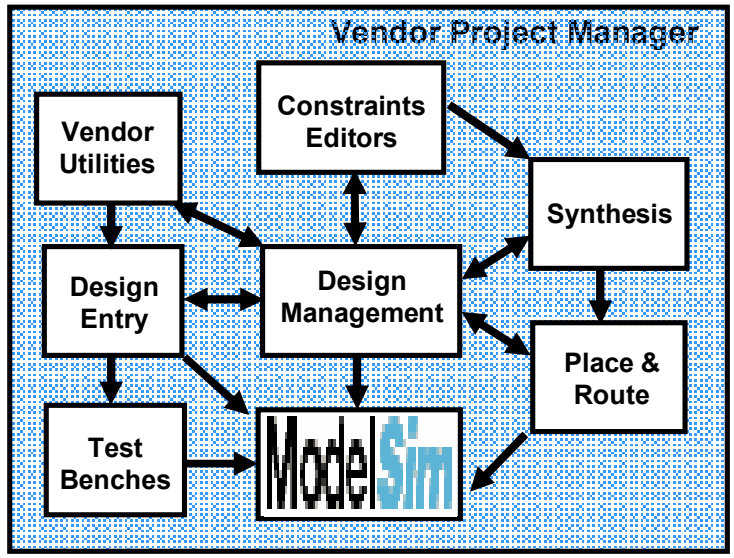
- User Defines In All Cases
  - Project Name, Base Directory Location and Default Library name
- Import Compile Script or Project File
  - Automatically Sets Project Name
  - Library Names extracted
    - From vlib commands or mpf file
  - Source Files extracted & Imported
    - From vcom/vlog commands or mpf file
- Generates MSD Script Based On MSD Project Command
  - Project new, Project addlib
  - Project addfile, Project compile



FPGA Vendor Mode



- Change ModelSim Executable Path In Vendor Tool
- Vendor Project Manager
  - Detects use of –do switch
  - Actel Libero Detects .prj file
  - Lattice ispLEVEL Detects .syn file
  - Xilinx ISE Detects .npl or .ise file
  - Uses compile Script Import Method

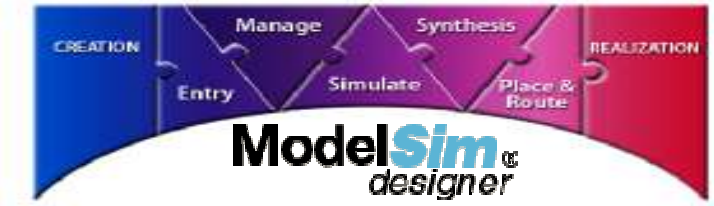


- Designer Used As Just Simulator
- Automatic
  - Creation Of Project
  - Keep Vendors Directory Structure, adds <library> directories
  - Import Source By Reference using .rlnk files in hdl directory
- Can Then Either Use Designer Functionality or Vendor

Agenda

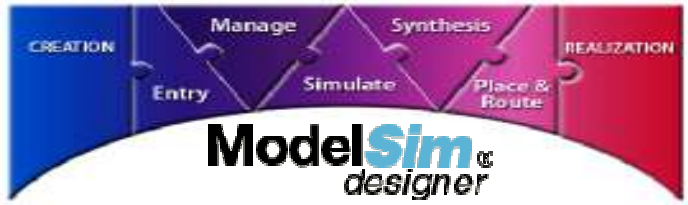
- Introduction
  - FPGA Design Flows
  - Vendor Tools
- ModelSim Designer
  - Features
  - **Packaging**
  - **Options**
- Product Demonstration

Product Packaging

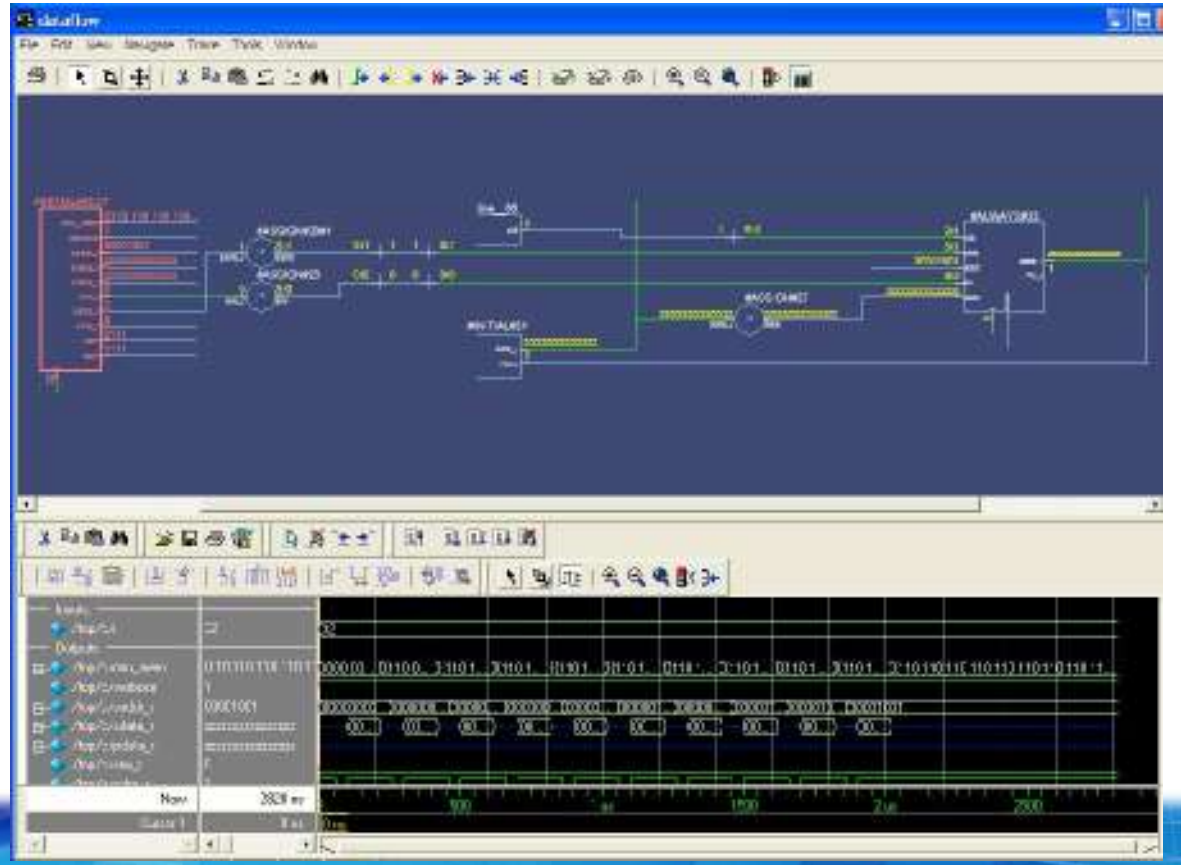


- **Product Configurations**
  - Single Language VHDL or Verilog
  - Dual Language PLUS Version
- **Licensing Options**
  - Node-locked or Floating
  - Standard Multiple Vendor Support
  - Windows Only
- **Extended Functionality Via Options**
  - Extended Dataflow
  - Waveform Compare
  - Code Coverage & Profiler
  - HTML Documentation
  - SWIFT Model Interface

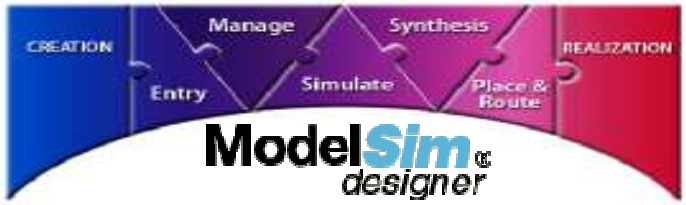
Extended DataFlow



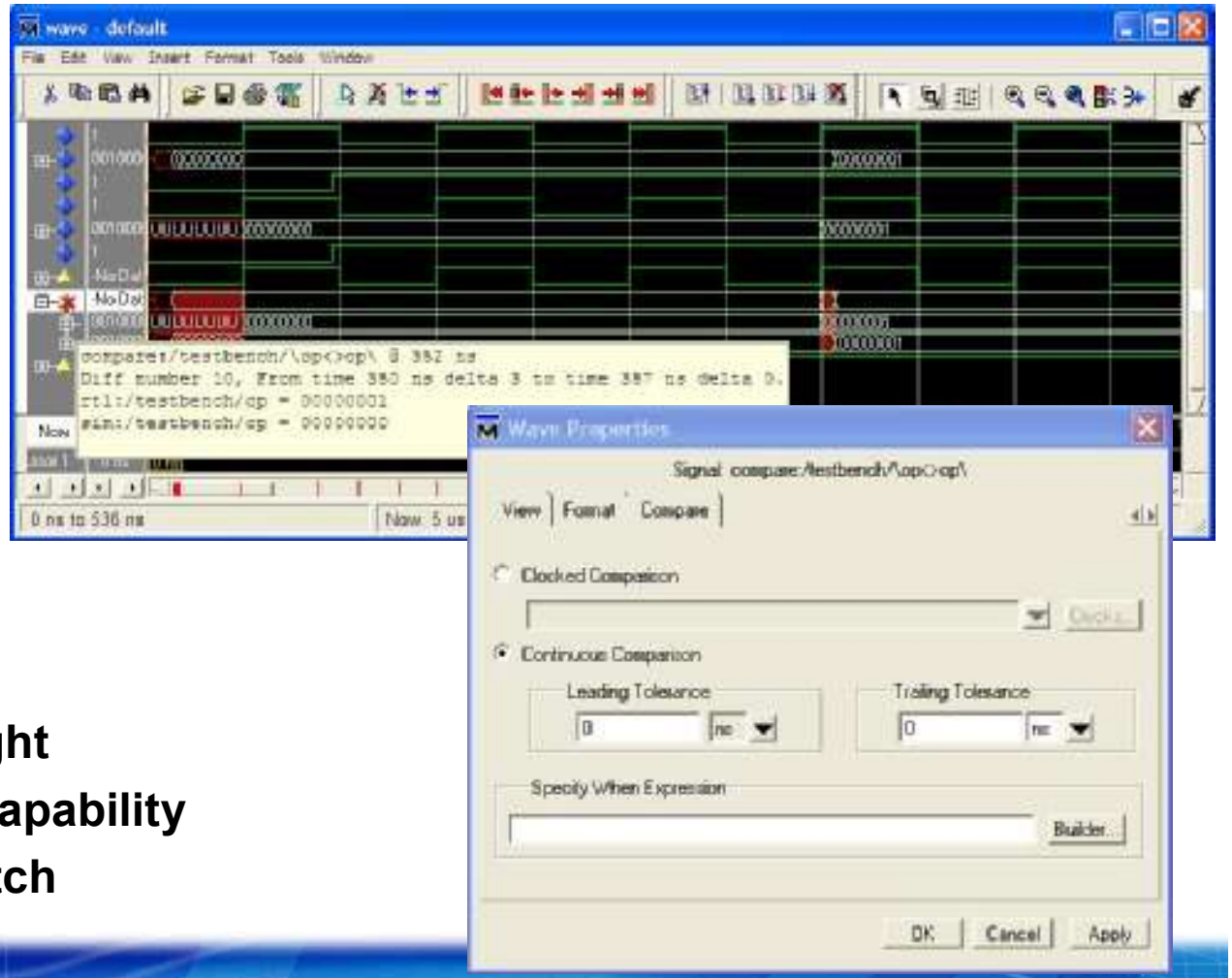
- Fast Visual Tracing From Cause To Effect
  - TraceX & ChaseX
- Tight Integration With All Simulation Windows
  - Drag ‘n’ Drop From Structure
  - Linked To Source
  - Values Tied To Wave Window Cursor
- Ease To Use
- Faster Debug
- Integrated Wave Display From Selected Object



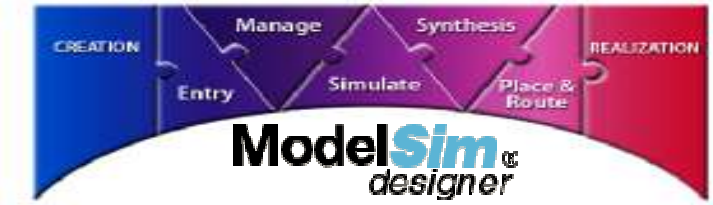
Waveform Compare



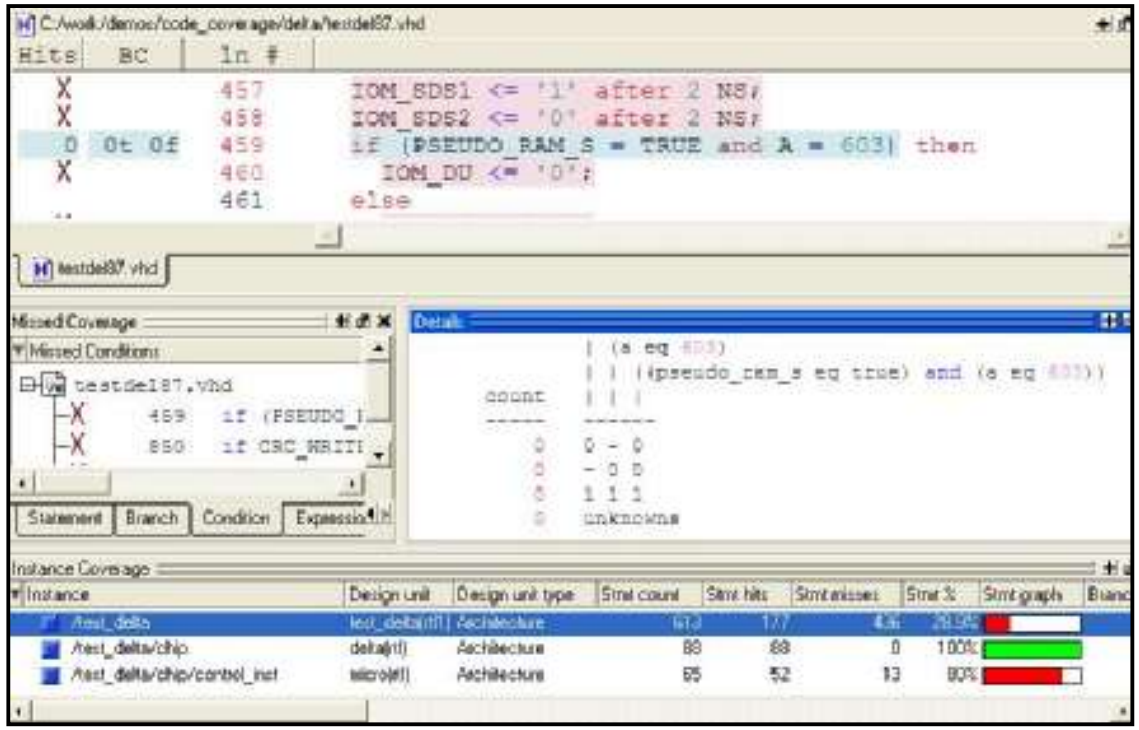
- Compare Multiple Simulation Runs To Golden Database
- Extremely Fast
  - WLF Binary
- Fully Configurable
  - Continuous
  - Tolerance
  - Clocked
  - Complex
- Easy to Use
  - Wizards
  - Totally Integrated
  - Scroll bars highlight
  - Powerful search capability
  - Text reports & Batch



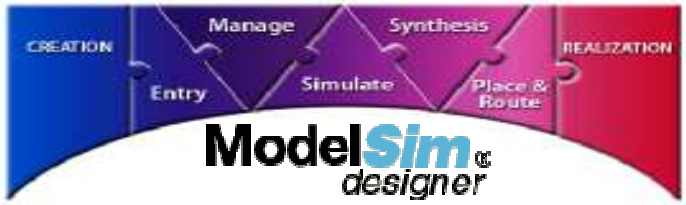
Code Coverage



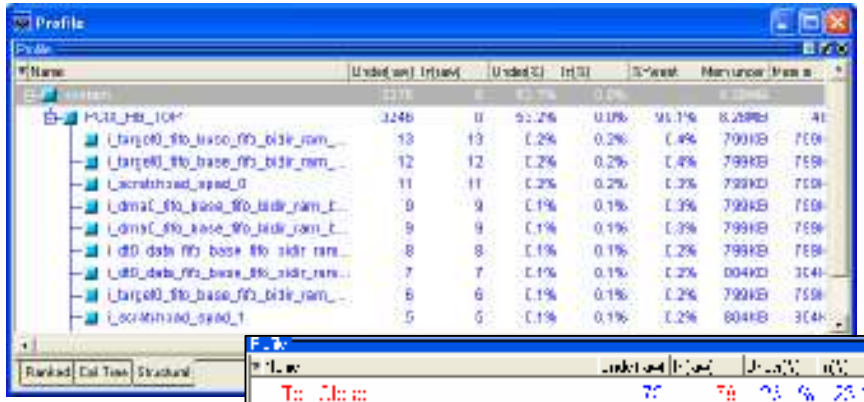
- **Measurement Of Code Execution**
  - Have I Tested All Of My Design ?
  - Optimize Unneeded Functionality
- **Supported Metrics**
  - Statement + Branch
  - Expression + Condition
  - Toggle
- **Fast Integrated GUI**
  - Source Annotation
  - Missed Coverage, Filtering, Detail Views
- **Flexible Reporting & Result Merging**

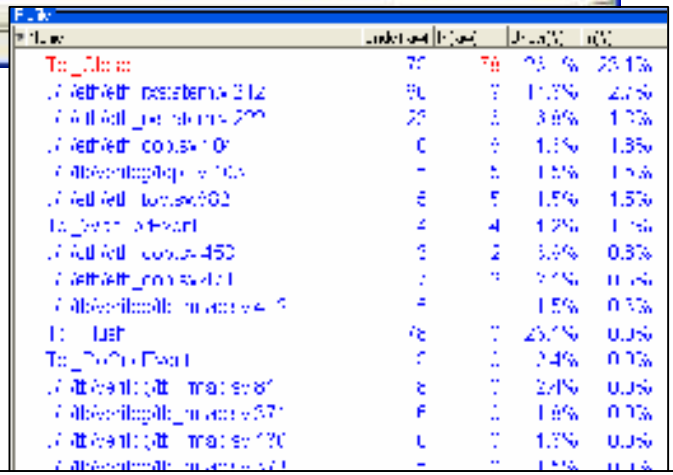


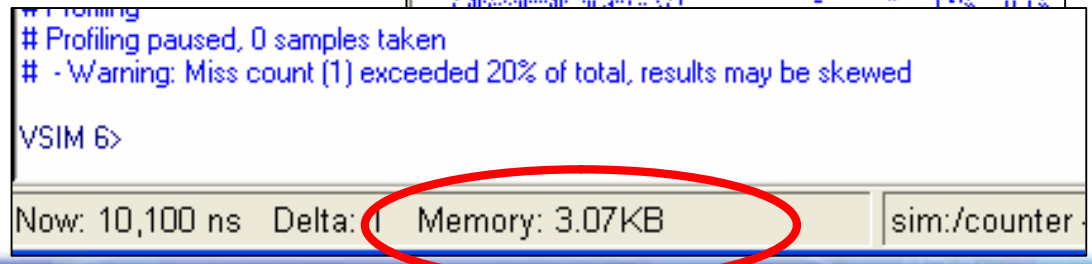
Profiler



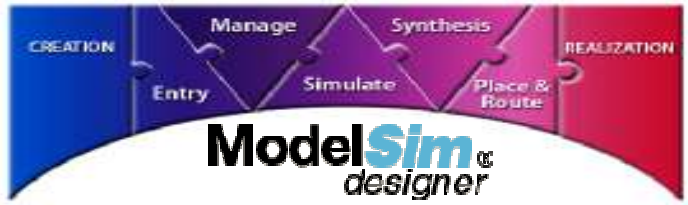
- **Performance Profiling**
  - **Reveals Simulation Run-Time Bottlenecks**
  - **Can Save Verification Time**
- **Memory Profiling**
  - **Finds Memory Intensive sections**
  - **Allows Larger Designs To Be Simulated**
- **Flexible Results Viewing**
  - **Linked To Source Code**
  - **Instance Based**
  - **Analyzes VHDL & Verilog & 3rd Party Tools**



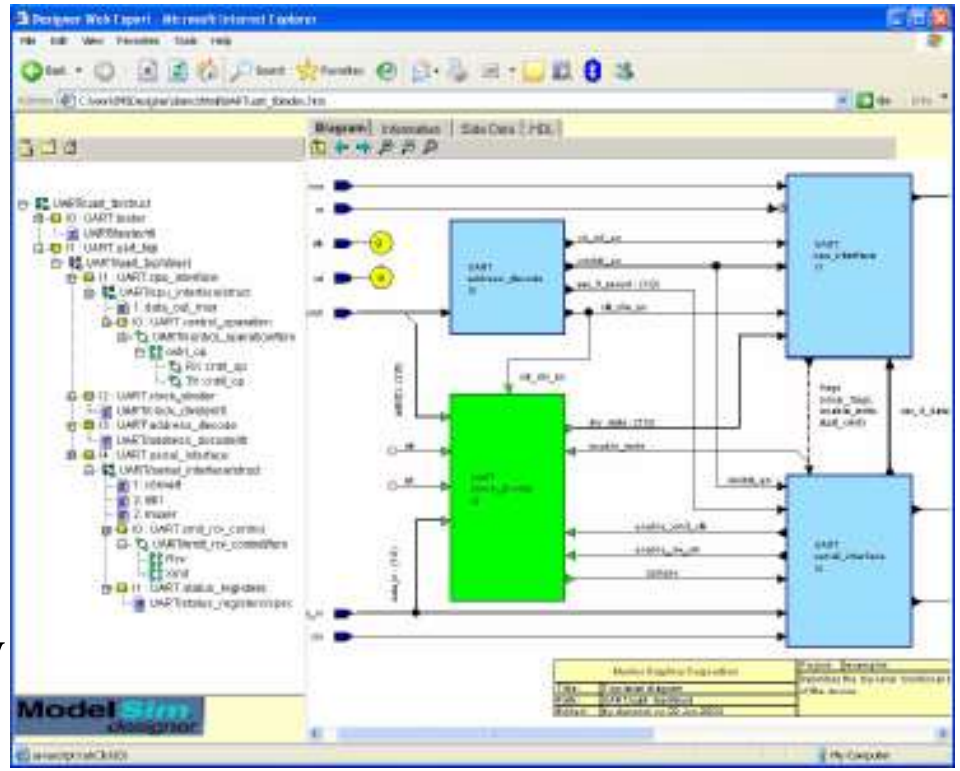




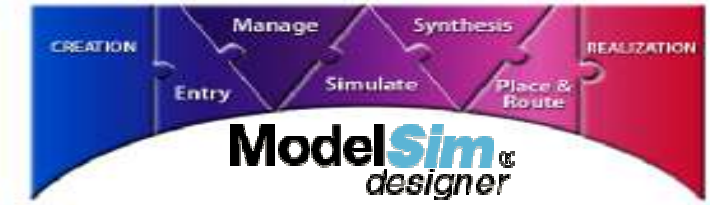
HTML Export



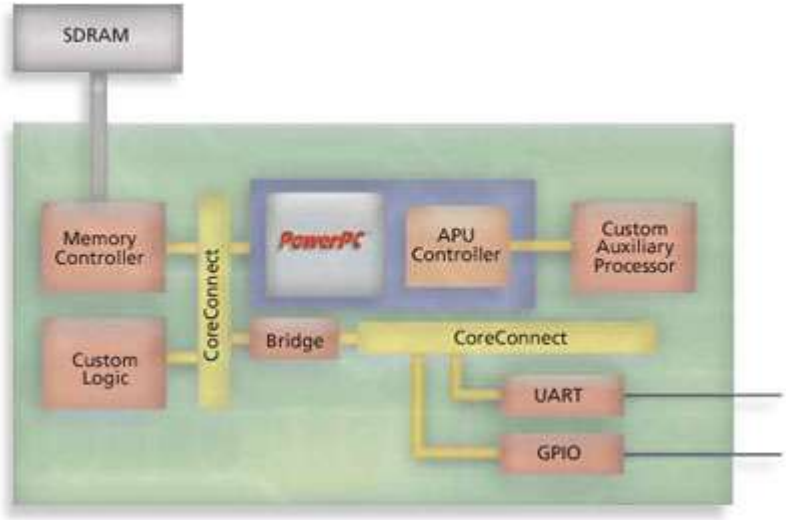
- Popular HTML format
  - Aids Communication
  - Design Reviewing And Understanding
- Export Complete Projects, Libraries, or Design Units
  - Graphical & HDL Code
  - Design Data
- Navigation
  - Hierarchical Structure View
  - Point And Click
- Flexible Output Options



SWIFT Interface



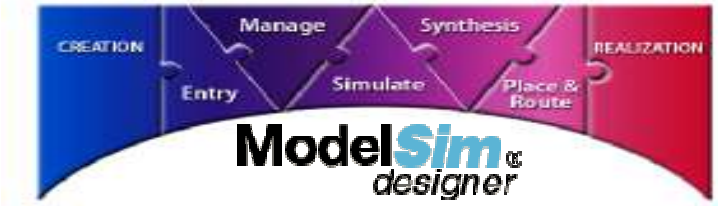
- Simulation Modeling Interface
  - Industry Standard
  - Complex Models & BF Models
- Xilinx
  - PowerPC
  - Gigabit I/O
- Altera
  - Excalibur and ARM Processors



ARM POWERED

EXCALIBUR™

ModelSim Value



- **Simple Single Environment**
  - Shortens learning curve
  - Reduces risk and cost
- **One tool manages it all**
  - One User Interface for everything
  - Single point for support
- **ModelSim Family Grows With Your Needs**
  - The brand name
  - Standards Based
  - Design size and complexity continues to increase
    - Lots of options available
    - ModelSim SE & HDL Designer Bundles
    - High-end Questa Functionality, ABV, SystemVerilog etc

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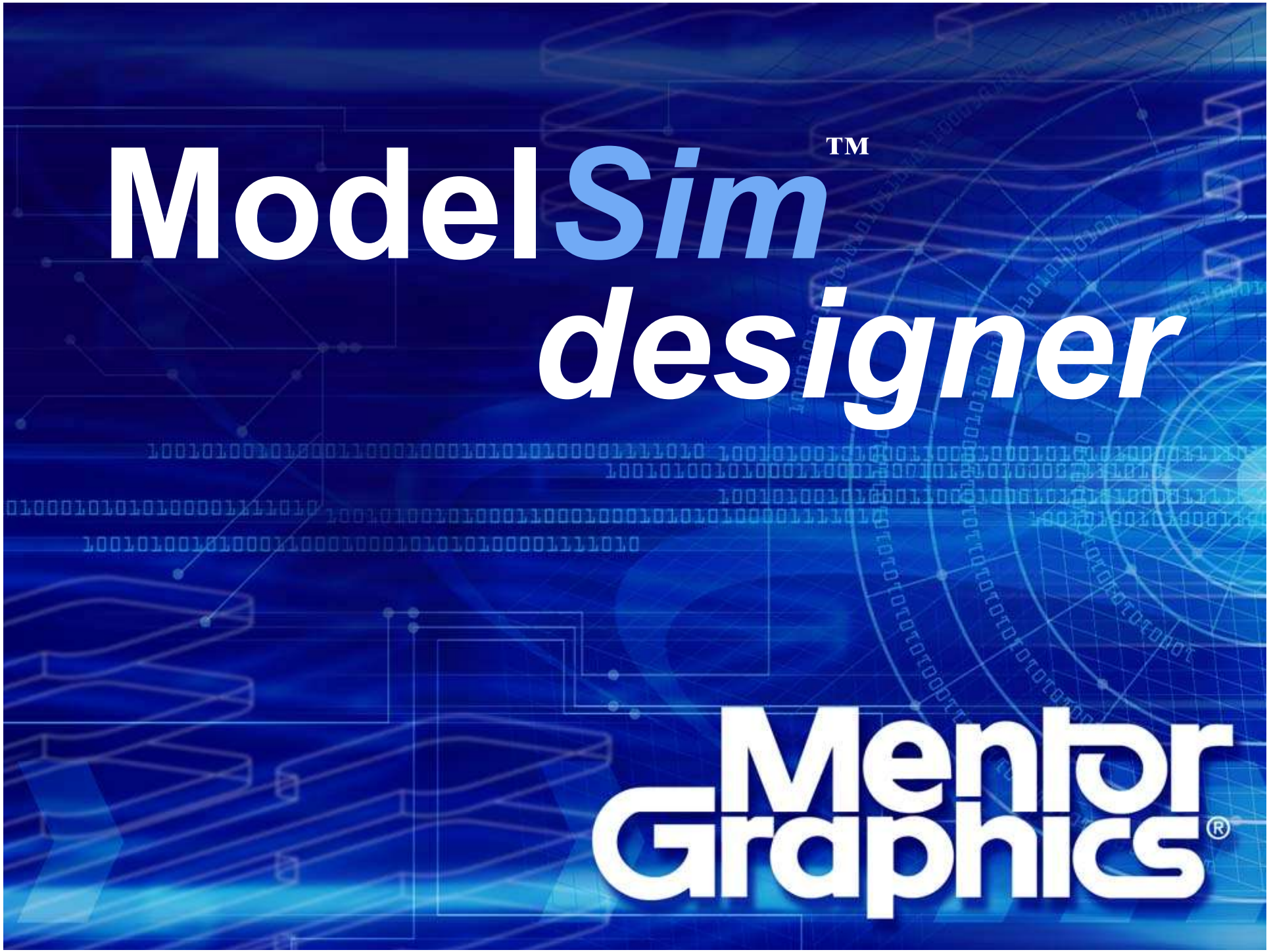
ModelSim™
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