

Introducing Mentor Graphics Brno CZ Oct.12, 2005

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HDL Channel Sales Manager EMEA

**Mentor
Graphics®**

What is Electronic Design Automation (EDA)?



- The Electronic Design Automation industry provides the design software used to create all of the world's electronic systems
- It is time-critical technology used to design the most complex system-on-chip(SoC) semiconductors & printed circuit boards
- Mentor Graphics has been an EDA industry leader for two decades with annual revenues over \$700 million

Mentor Graphics

Focused on Growth Segments of EDA

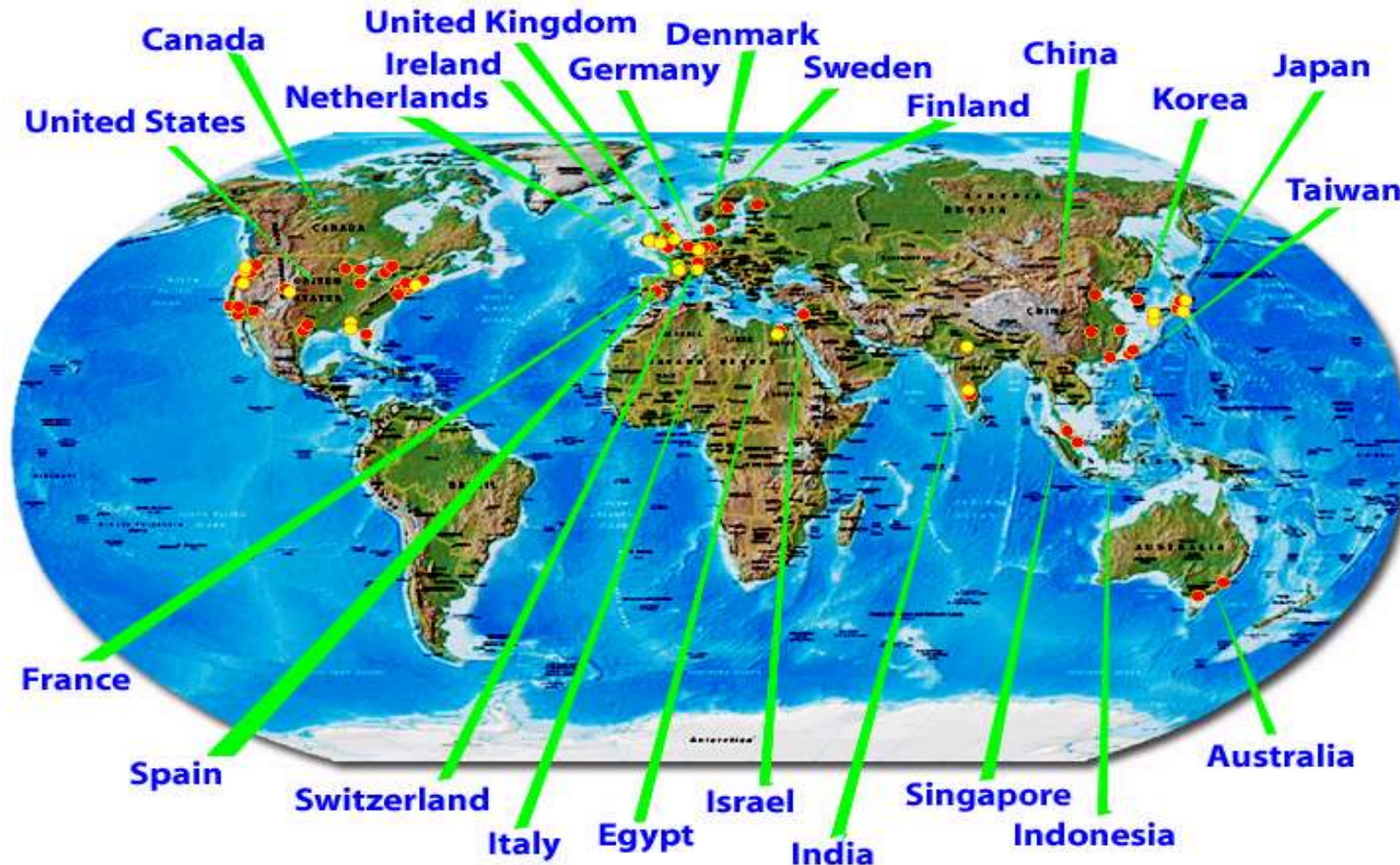


- Revenue - over \$711 million in 2004
- Worldwide market share ~19%
- Fastest growing major EDA company*

Note: *Five year CAGR

Mentor Graphics Around the World

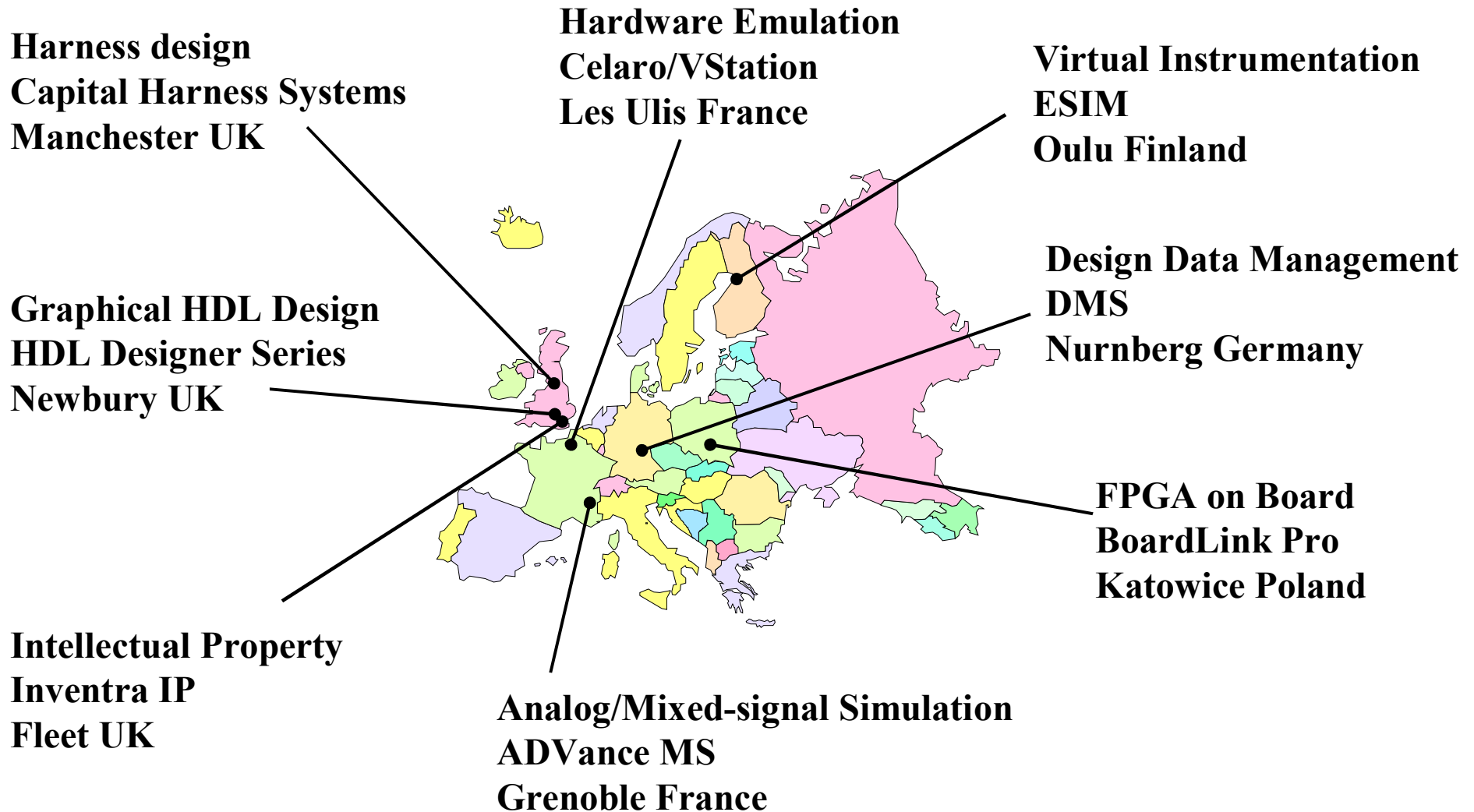
Operates through 28 engineering sites and 52 sales offices around the world



● Key Sales Offices

● R&D Sites

Mentor Graphics European R&D

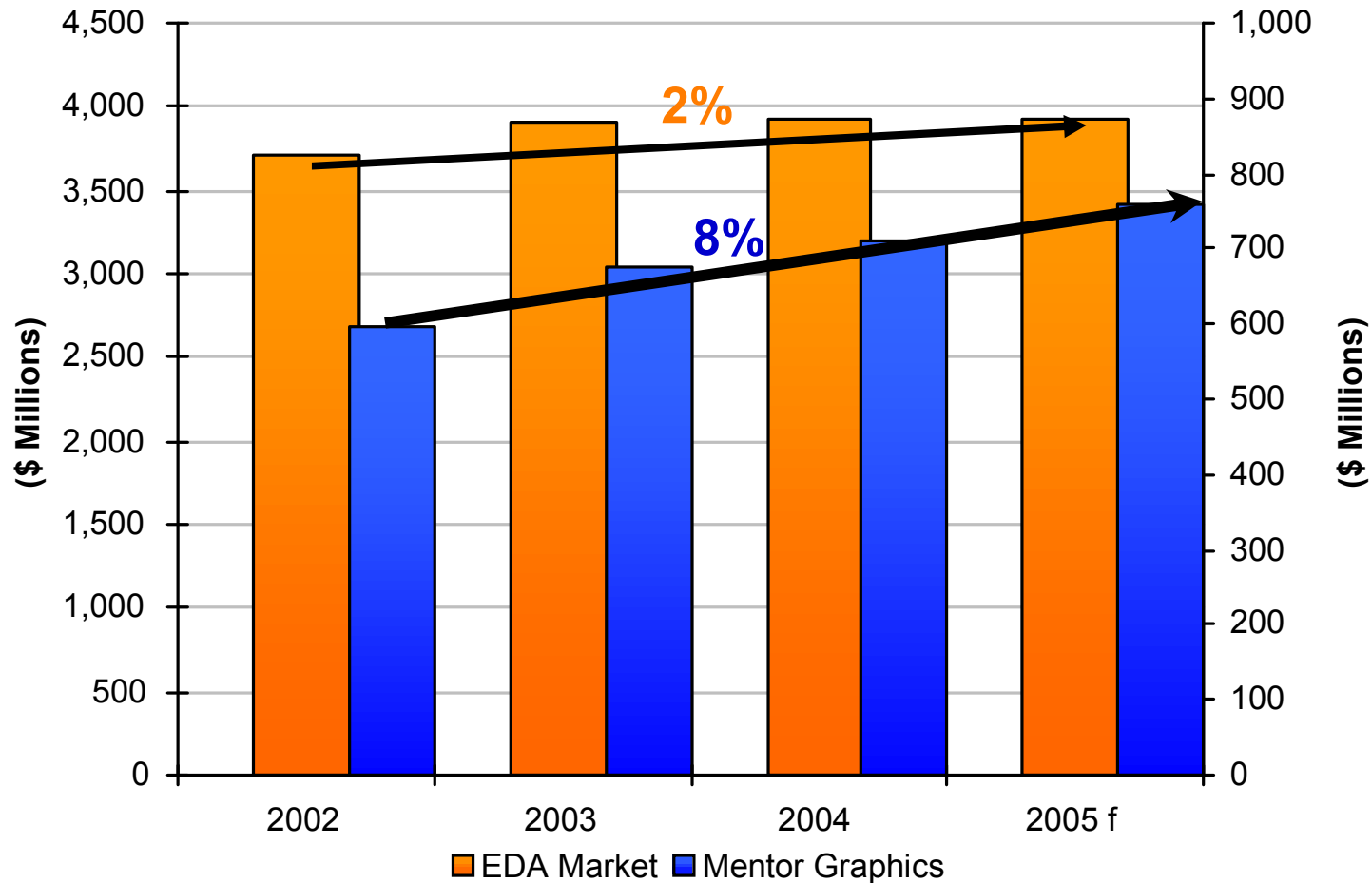


Mentor Graphics Europe



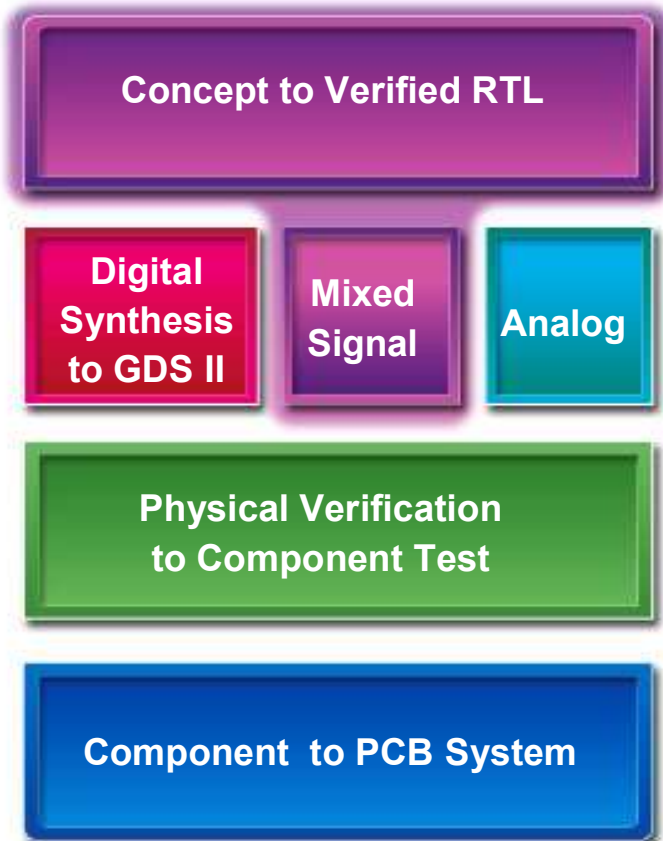
- **~800 employees (60% engineers)**
- **Four geographic regions**
- **Numerous field offices**
 - **Finland, Israel, Egypt, Grenoble...**
- **Strong Distribution Network for HDL and PCB**
- **>30% of MGC WW revenue**
- **Europe Market share / Dataquest**
 - **Total EDA 24.6%, PCB 51%, CAE 26%**

Mentor vs. the EDA Market



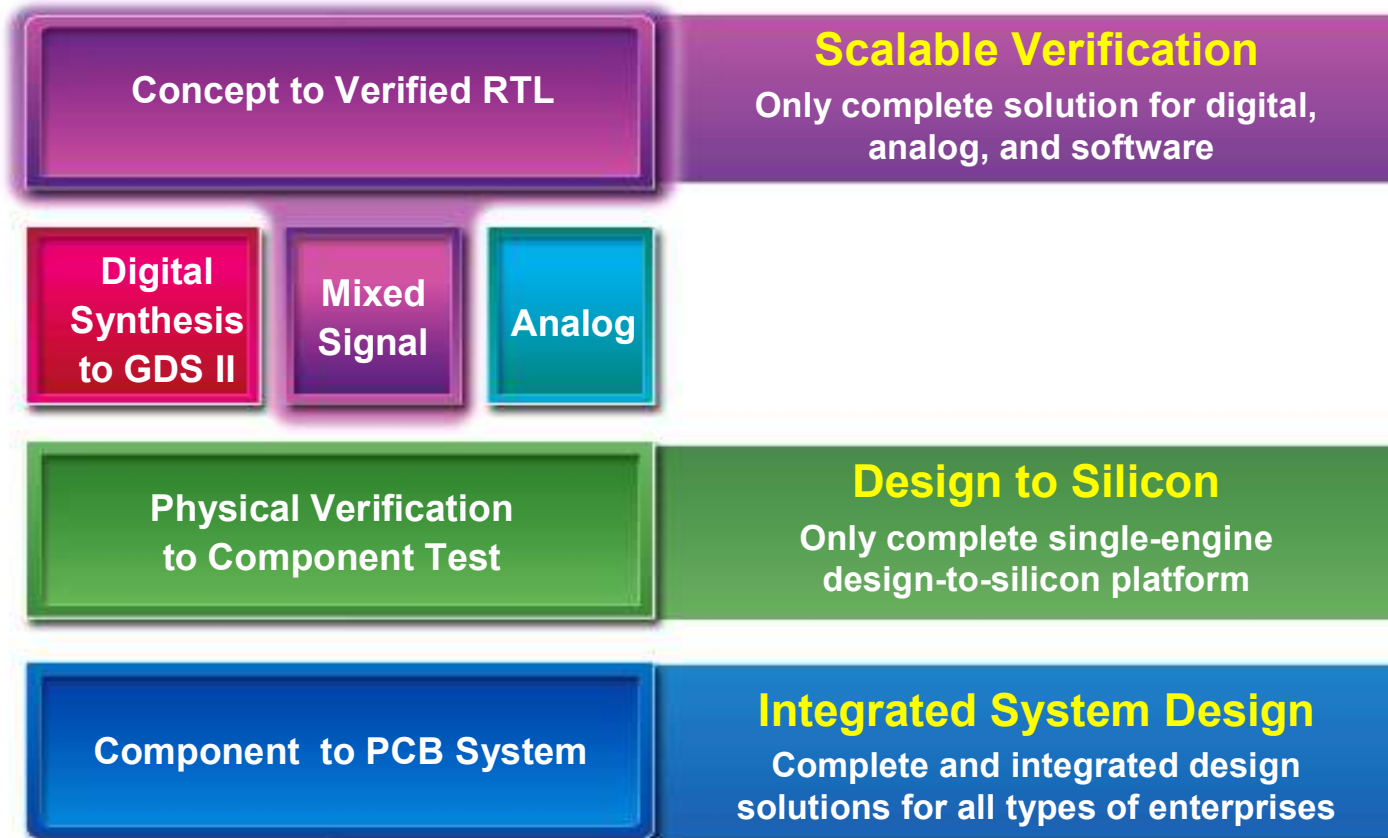
Source: EDAC Market Statistics, Company Reports, Financial Analyst Reports, Mentor Estimates

Mentor Strategy

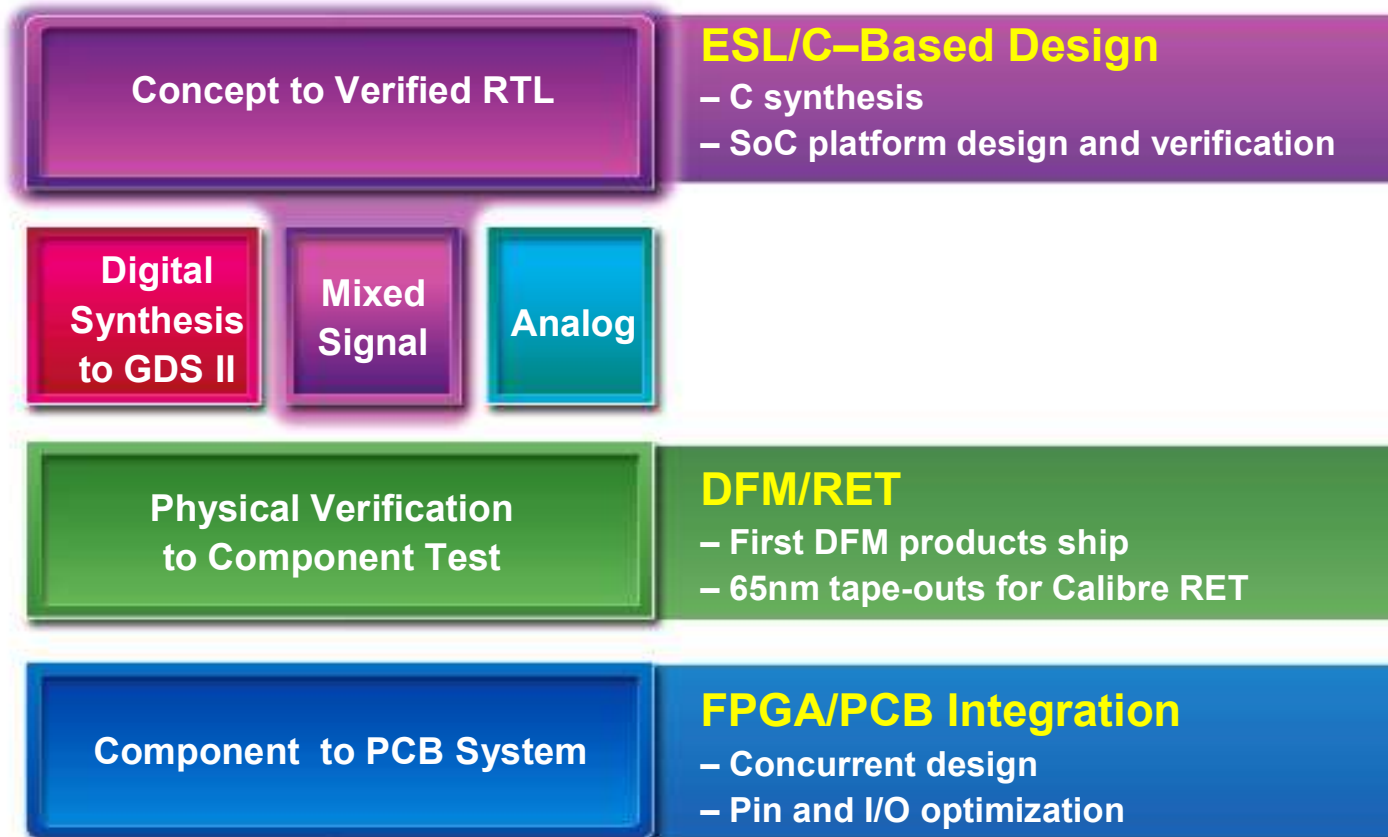


- **Focus on leading platform solutions where we:**
 - Add significant value for designers
 - Bring innovative technology
- **Develop adjacent markets for additional growth**
 - Embedded software
 - Automotive electronics
 - IP and reuse

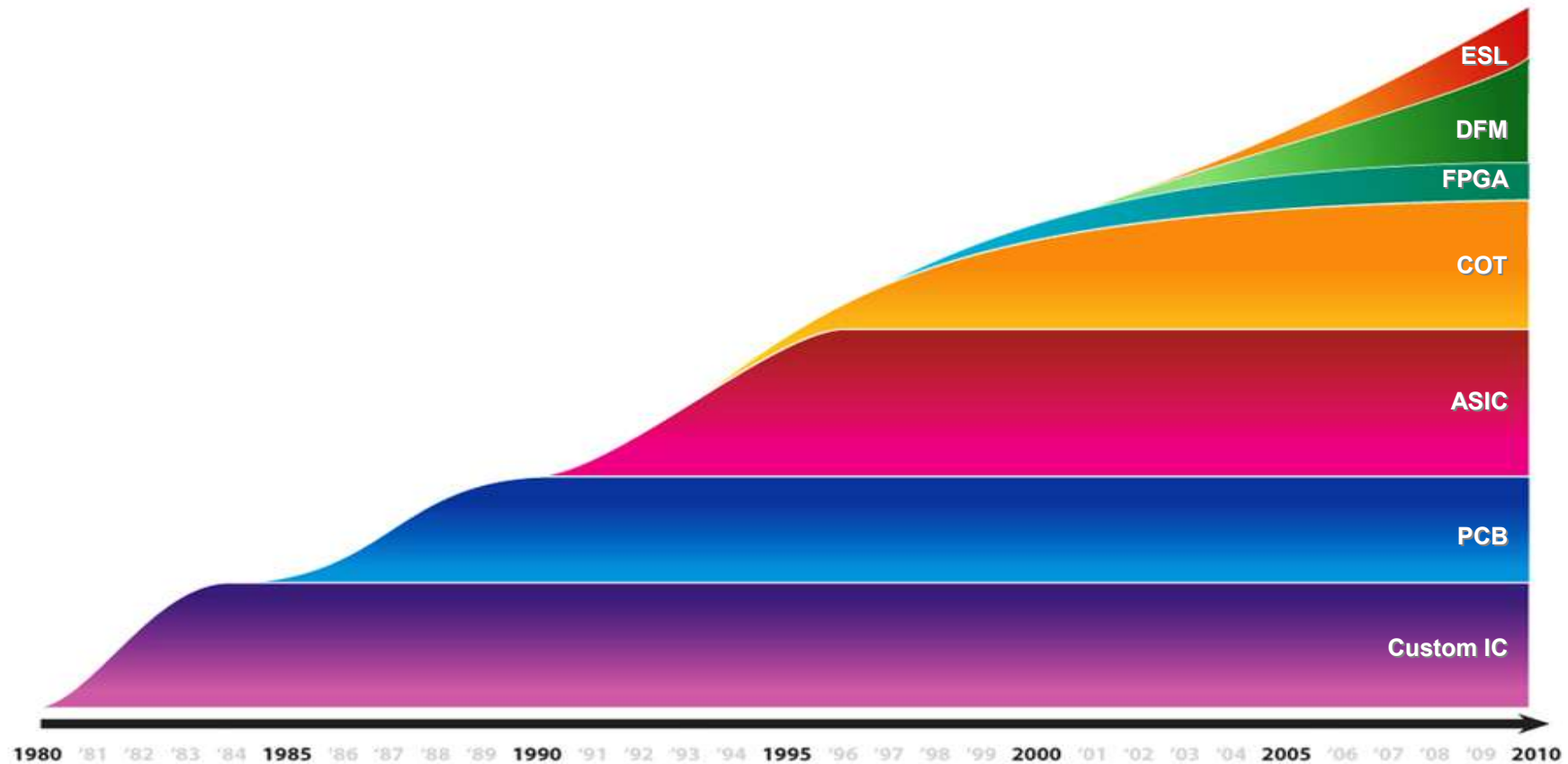
Mentors Leading Platform Solutions



Mentor's Success in New Growth Areas

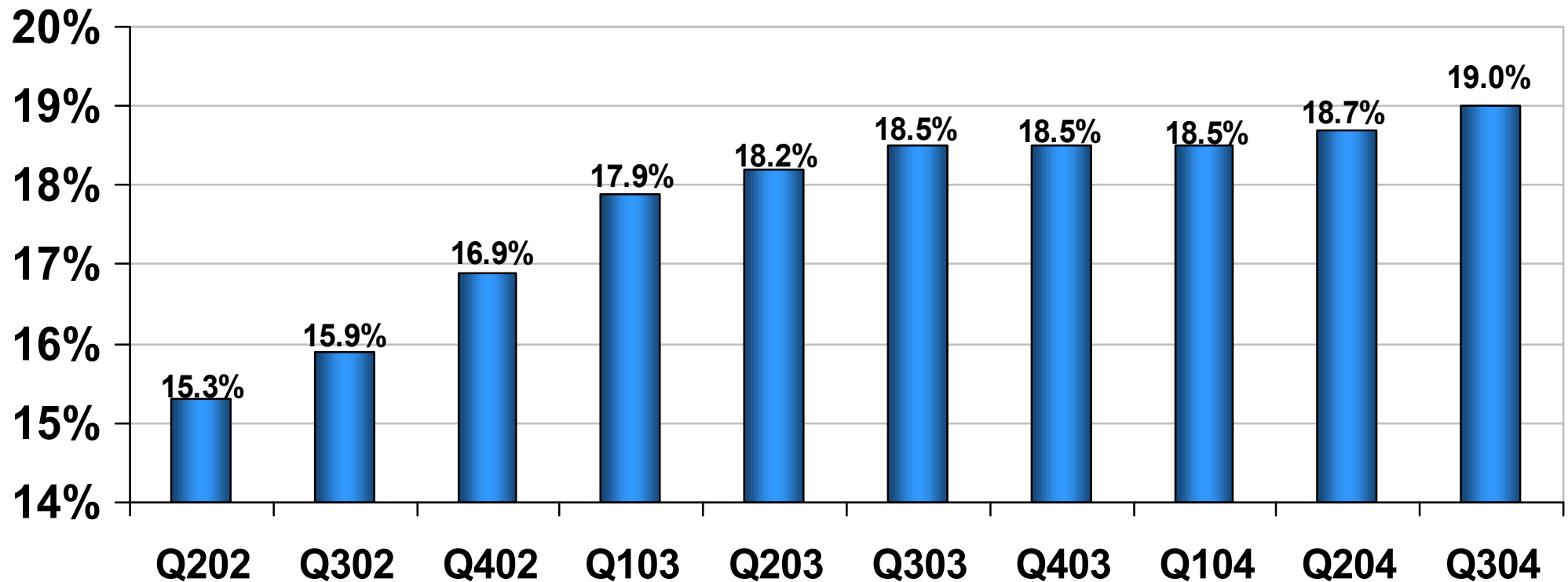


Investing in Major New Design Methodologies



Focus on #1 Positions Drives World Wide Market Share Gains

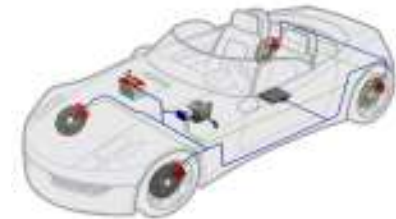
Mentor Graphics License & Maintenance Market Share
(Rolling 4 Quarters)



Source: EDAC Market Statistics Excluding SIP

Developing Adjacent Markets

- **Automotive Electronic content: 23% of new car price/ 40% by 2010**
- **Average new car contains 25 Microcontrollers (MCUs)** IC Insights
 - **Luxury vehicles contain up to 80 MCUs**
- **Mentor: Harness design, system simulation & analysis**



Wire Harness

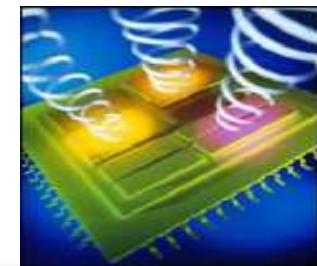


Embedded Software

- **Convergence of SW & HW design**
- **Software now key consideration for many designs**
- **Mentor: Embedded SW solutions, co-verification**

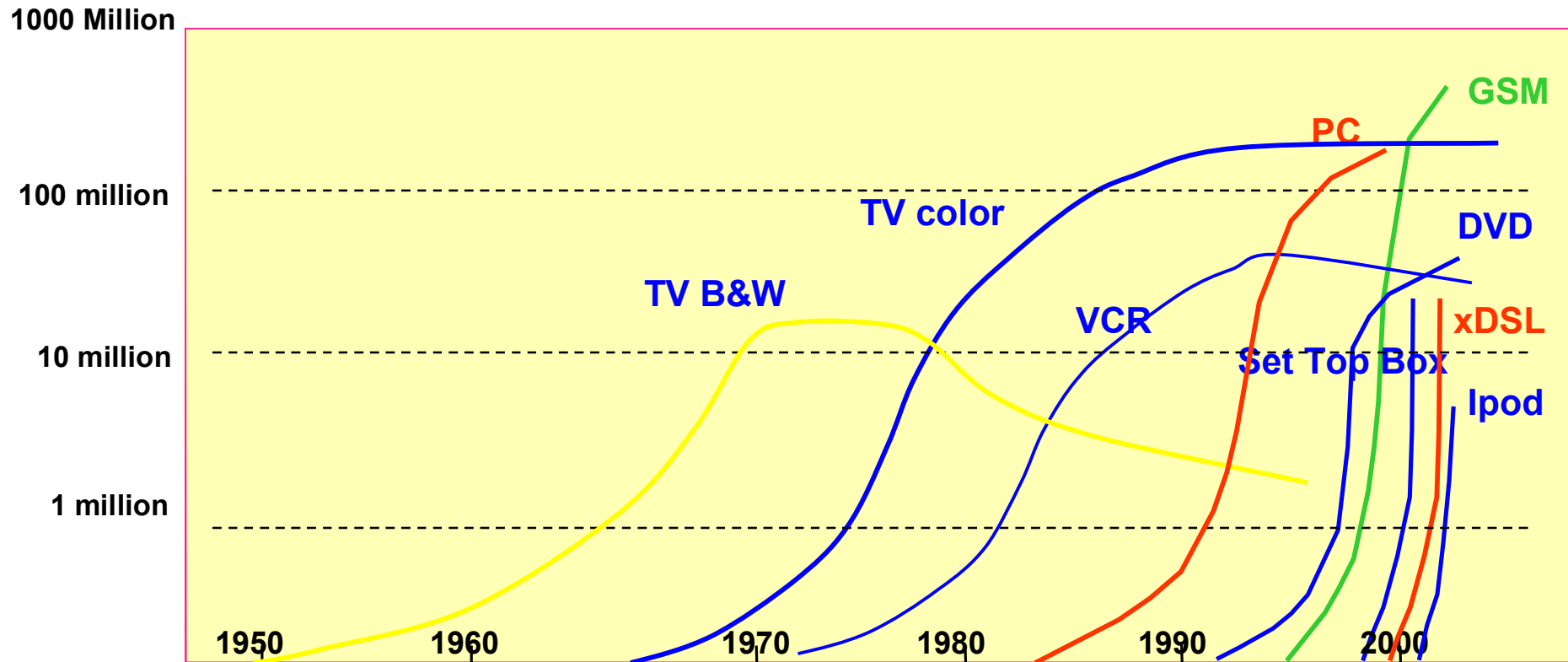
- **Reuse increasing, Average ASIC contains 17 Blocks** Collett Int.
- **IP important for productive SoC and FPGA design**
- **Mentor: portfolio of key IP and services (USB, SATA, Ethernet...)**

Intellectual Property



Time to Market: Increasingly Important

Acceleration of Mass Markets

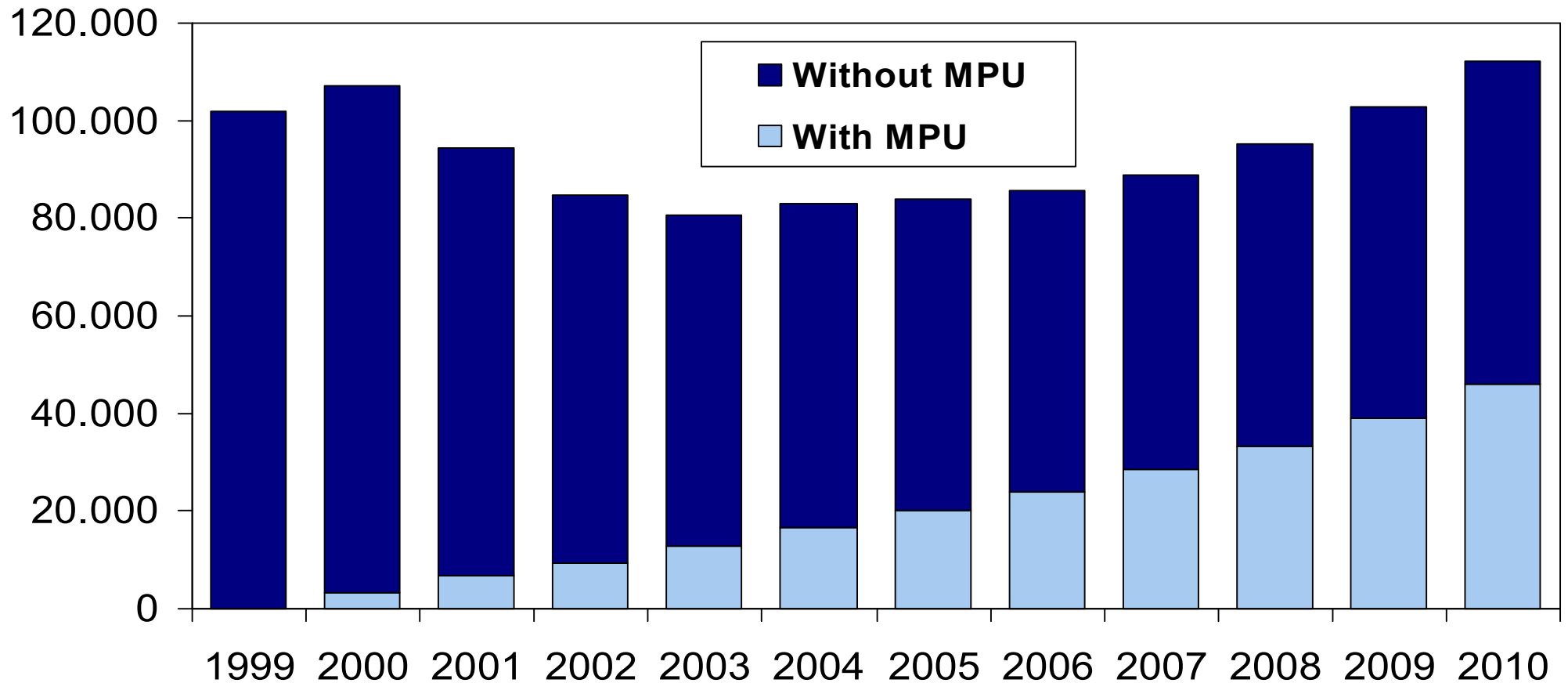


No second chances if markets are missed

Source: Gartner & STMicro

FPGAs Dominate Design Starts

Number of FPGA/PLD Design Starts



Source: Gartner June 2005

FPGA Addresses Design Issues

Time to Profit Issues

- Shorter Design Cycle
- Return on Investment
- Risk Management
- Higher Complexity
- Higher Performance
- Evolving Standards
- Product Differentiation
- Customer Service

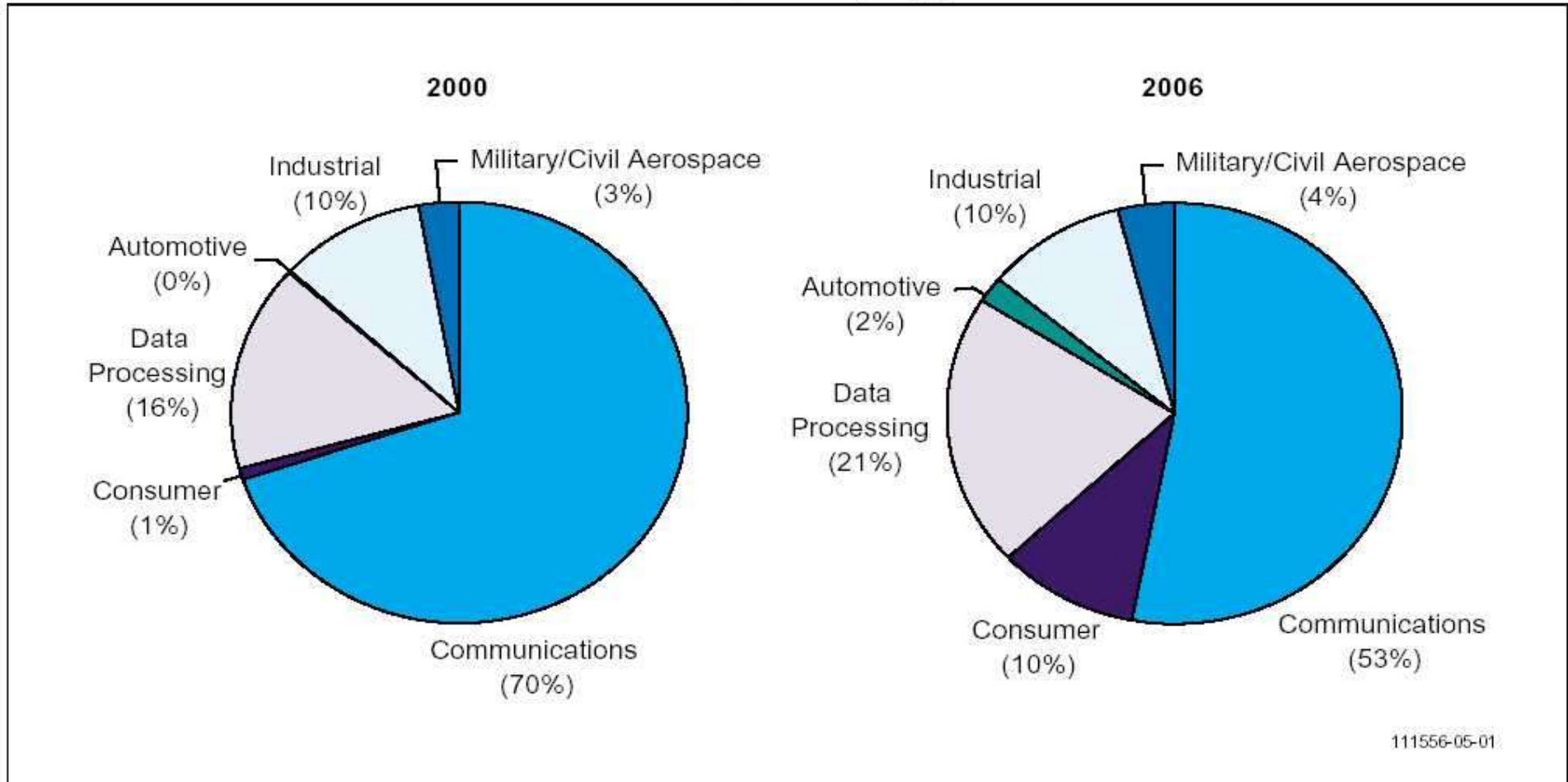
FPGA Features

Time-to-Market
Low Development Cost
(Re) Programmability
Reuse / IP
Leading-Edge Technology
Flexibility
Customisable Solution
Field Upgradability

Source: Altera

WW FPGA Applications

Estimated Worldwide FPGA/PLD Consumption by Application Market, 2000 and 2006



Source: Gartner Dataquest (November 2002)

Interoperability Improves Productivity

- Deep integration between design capture, simulation, synthesis, and place & route enhances debugging and improves overall design time

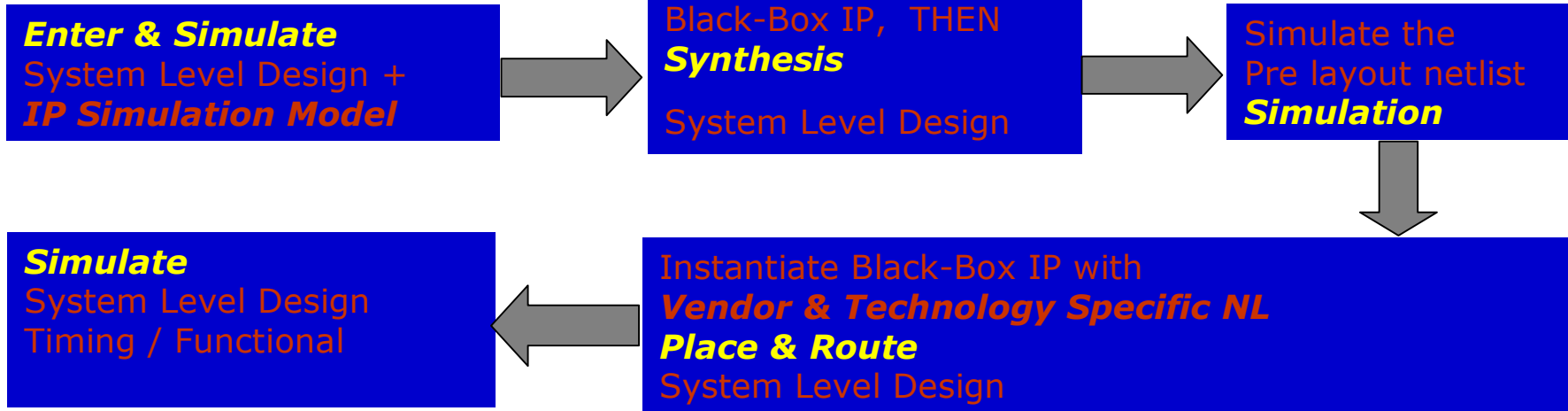


FPGA Design Flow

HDL Designer, HDL Author
 Modelsim Designer
 FPGA Advantage

Leonardo L2& L3
 Precision
 FPGA Advantage

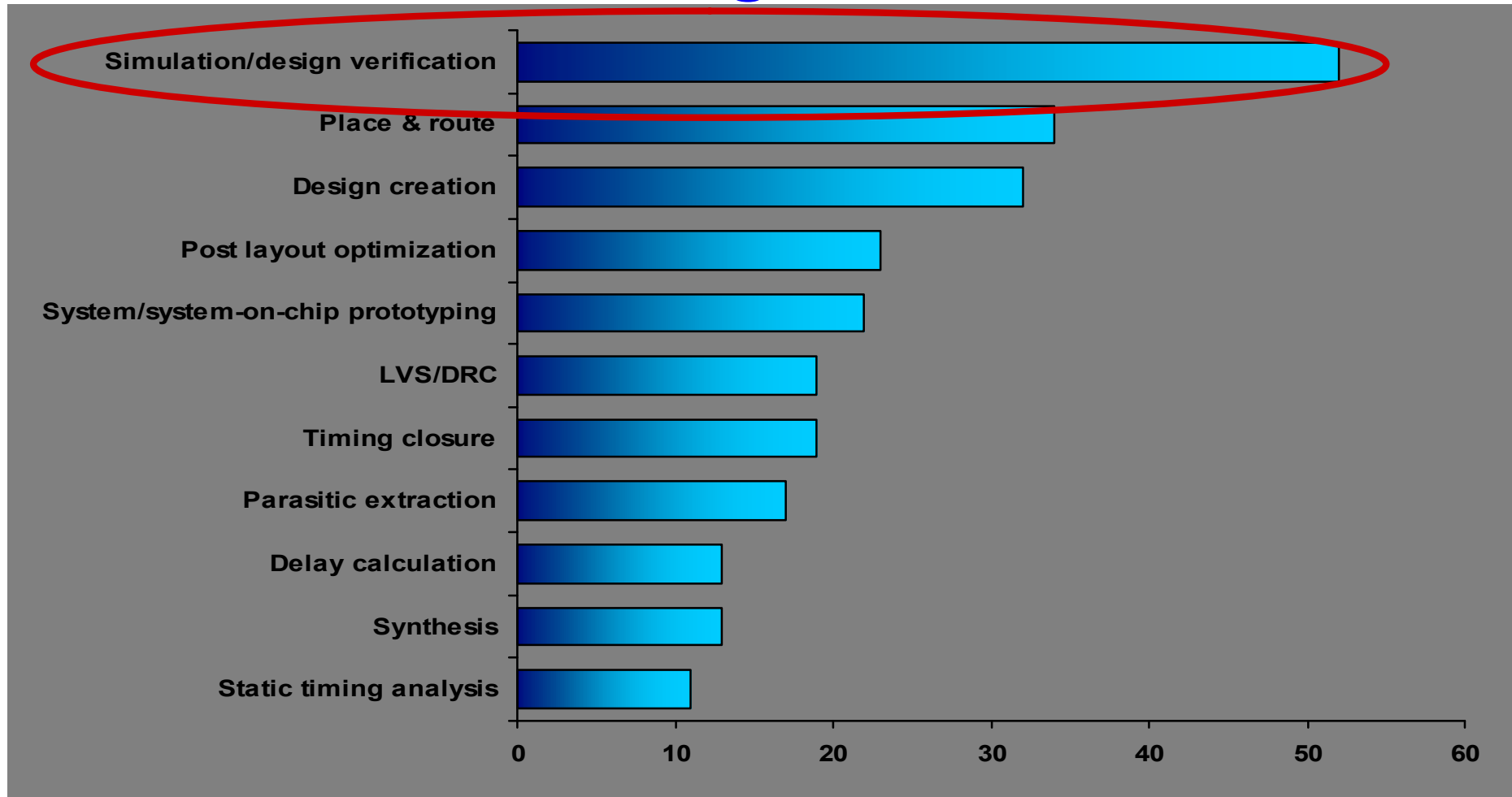
Modelsim Designer
 Modelsim PE & SE
 FPGA Advantage



Modelsim Designer
 Modelsim PE & SE
 FPGA Advantage

Altera –Quartus
 Xilinx –ISE
 Actel - Libero
 Lattice – ISP Lever

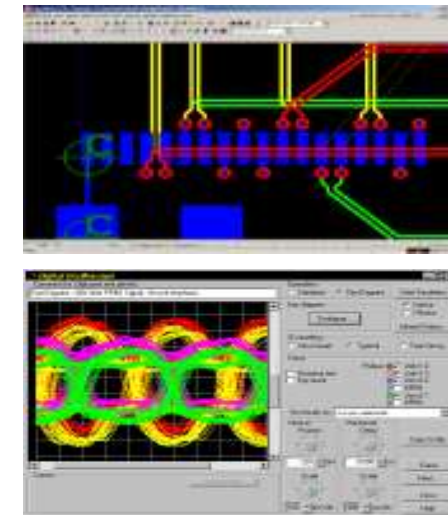
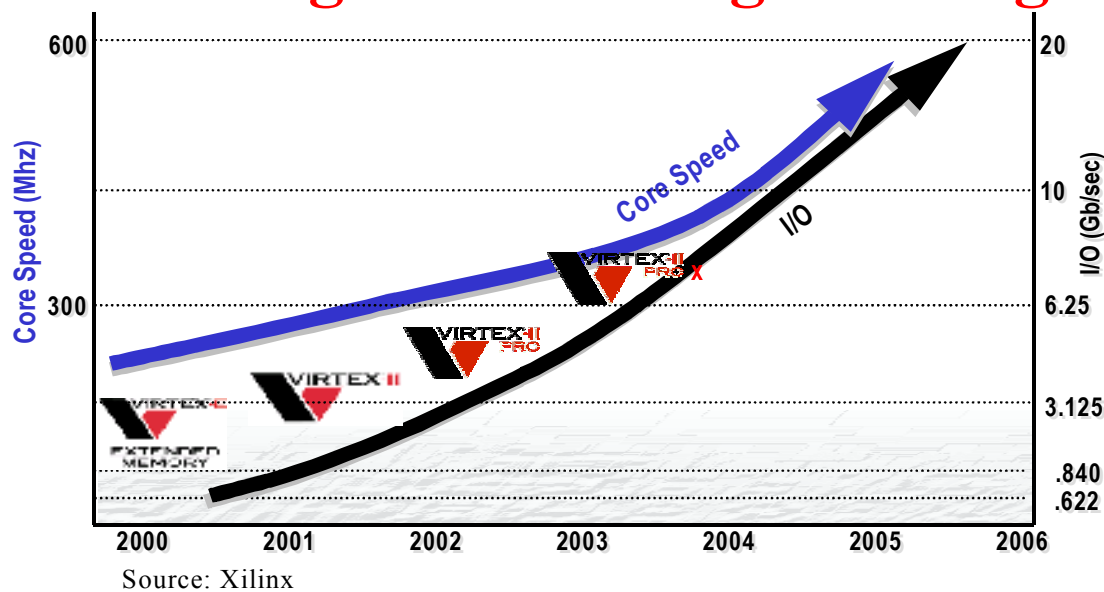
Percentage of Areas Described as Bottleneck in Design Flows



Sources: EETimes and Enterprise Planning & Research Ltd., Pan European Independent Survey Q2 2001

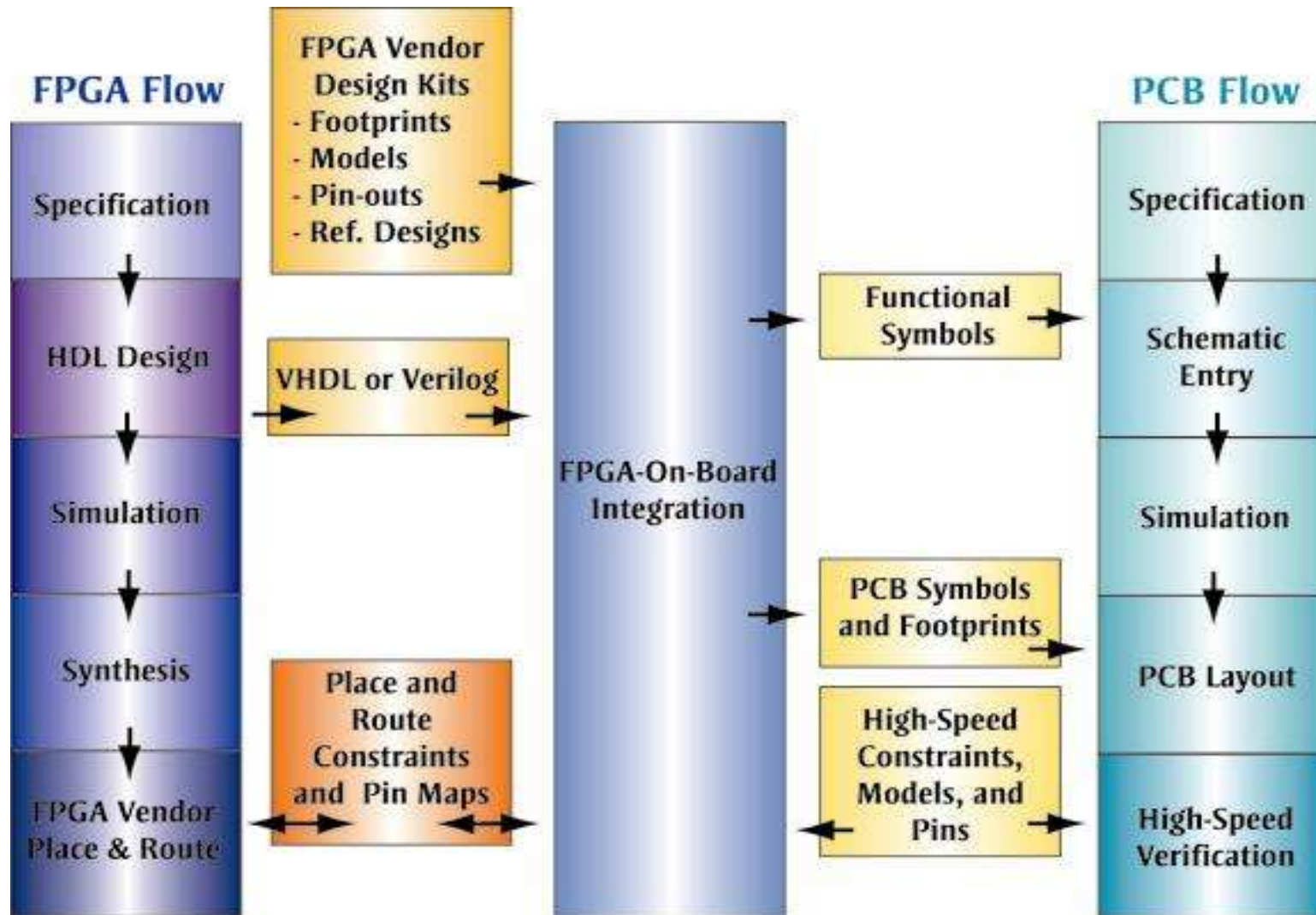
Challenge: FPGA to Board Interface

- FPGAs now using 3rd generation I/O (3GIO) inter-chip serial communication up to 10 giga-bits per second
- PCB solution must have:
 - **Finely tuned differential pair routing**
 - **Next generation Signal Integrity Analysis**



Multi-Gigabit Signal Integrity Analysis

Mentor's Integrated Systems Design



Strongly Positioned in Current EDA Growth Segments and Emerging Markets

- **Leading technology platforms**

Scalable Verification, Design to Silicon, Integrated Systems Design

- **New methodologies**

ESL/C-Based Design, DFM/RET, FPGA/PCB Integration

- **Adjacent markets**

Wire Harness, Intellectual Property, Embedded Software

- **Serving customers**

Leading products and award winning support

EDN 'Image & Market Measurement' EDA Survey Q303

	No.1	No.2	No.3
Technology Leadership	Cadence	Mentor Europe	Synopsys
Customer Orientation	Mentor Europe	Cadence	Synopsys
Good Business Practises	Mentor Europe	Cadence	Synopsys
Technology Vision	Cadence/Synopsys		Mentor Europe
Understands Customer Need	Mentor Europe	Cadence	Synopsys
First To Market	Synopsys	Cadence	Mentor Europe
Customer Support	Mentor Europe	Cadence	Synopsys
Quality & Reliability	Mentor Europe/Cadence		Synopsys
Low Price Leader	Synplicity	Cadence	Mentor Europe
Most Accessible	Mentor Europe	Cadence	Synopsys
Most Credible	Mentor Europe	Cadence	Synopsys
Market Leader	Cadence	Mentor Europe	Synopsys
Tool Perfection	Synplicity	Mentor Europe	Cadence/Synopsys

- Blind European survey, 357 respondents equally spread over Europe
- 23% IC, 25% FPGA, 35% PCB, 41% System designers
- “Highest image/awareness performance ever seen by I&MM consultants”



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www.mentor.com