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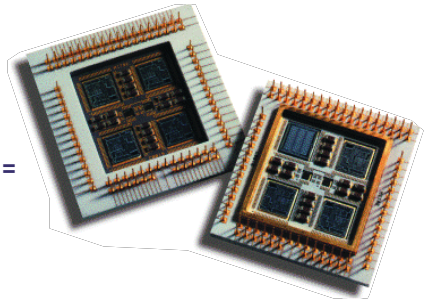

# ACUART IP CORE
# UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

ASICore FOR USE IN SoC

## BASIC PARAMETERS

- fully compatible with most common UART - 16550 (run in 16450 or 16550 mode)
- Receiver and Transmitter FIFOs each holding up to 16 characters (depth of FIFOs could be simply changed to meet customer's needs), time-out and trigger level indications for Receiver FIFO
- prioritized interrupt system
- two signals for DMA support
- modem handshake signals support with loopback diagnostics
- extensive possibilities of data format setup:
  - character lengths 5, 6, 7 or 8 bits
  - parity selection (none, even, odd, sticky)
  - 1, 1.5 or 2 stop bit lengths
- baud generator with 16-bit programmable divisor
- serial line errors protection including unstable start-bit detection
- transmission errors detection including break, frame, overrun and parity error

## FEATURES

Fully synthesisable HDL macro
Technological independenence
Complexity aprox. 7.5K gates

## DELIVERABLES

- Design file formats
  - RTL VHDL synthesisable code
  - Netlist
- Technical documentation
  - Data sheet
  - Design description document
  - Verification effort document
- Verification
  - Testbench
  - FPGA prototyping board
- Design tools scripts
- Maintenance

The ACUART is a soft core. The customer obtains documented VHDL sources of design and testbench. Documentation includes the Verification environment description and the User's Guide with detailed description of the ACUART functions, core verification and synthesis process. Unix scripts for design compilation, verification, synthesis and P&R are also available.

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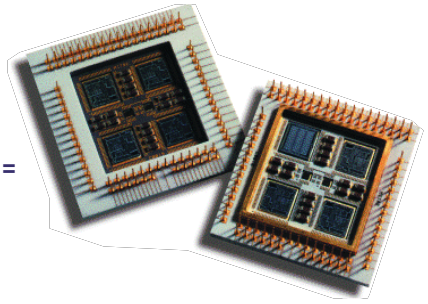
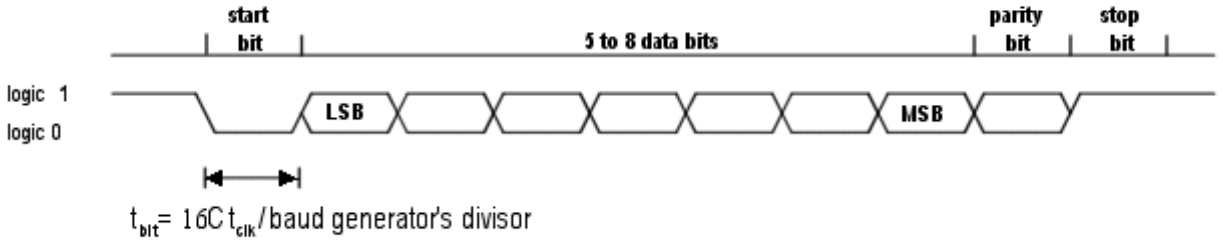


## BRIEF FUNCTIONAL DESCRIPTION

The ACUART utilizes the standard serial asynchronous communication protocol:




The system (host) uses the registers of the ACUART to read and write data, get and set transmission parameters, control modem handshake signals, enable/disable interrupts, program divisor of the Baud Generator and to perform other operations with the ACUART.

## ACUART PINOUT

| Port name | Direction | Description | Port name | Direction | Description |
|---|---|---|---|---|---|
| res | Input | Asynchronous reset, active high | nrxrdy | Output | Receiver ready DMA signal |
| clk | Input | System clock | ntxrdy | Output | Transmitter ready DMA signal |
| d[7..0] | Input/Output | Bidirectional data bus | sin | Input | Serial input |
| a[2..0] | Input | Address bus | sout | Output | Serial output |
| nads | Input | Address and chip select latch signal, active low | nbaudout | Output | 16x baud rate clock |
| cs0 | Input | Chip select, active high | nrts | Output | Request to send, modem handshake signal |
| cs1 | Input | Chip select, active high | ndtr | Output | Data terminal ready, modem handshake signal |
| ncs2 | Output | Chip select, active low | nout1 | Output | User output 1, modem handshake signal |
| rd | Input | Read data from the ACUART, active high | nout2 | Output | User output 2, modem handshake signal |
| nrd | Input | Read data from the ACUART, active low | ncts | Input | Clear to send, modem handshake signal |
| ddis | Output | External data bus driver control signal | ndsr | Input | Data set ready, modem handshake signal |
| wr | Input | Write data to the ACUART, active high | ndcd | Input | Data carrier detect, modem handshake signal |
| nwr | Input | Write data to the ACUART, active low | nri | Input | Ring indicator, modem handshake signal |
| intr | Output | Interrupt signal | | | |

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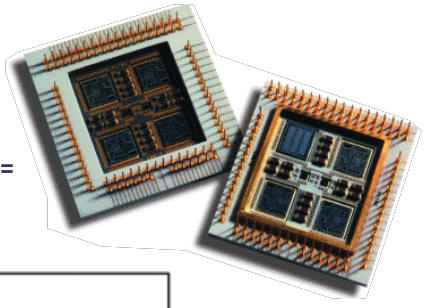


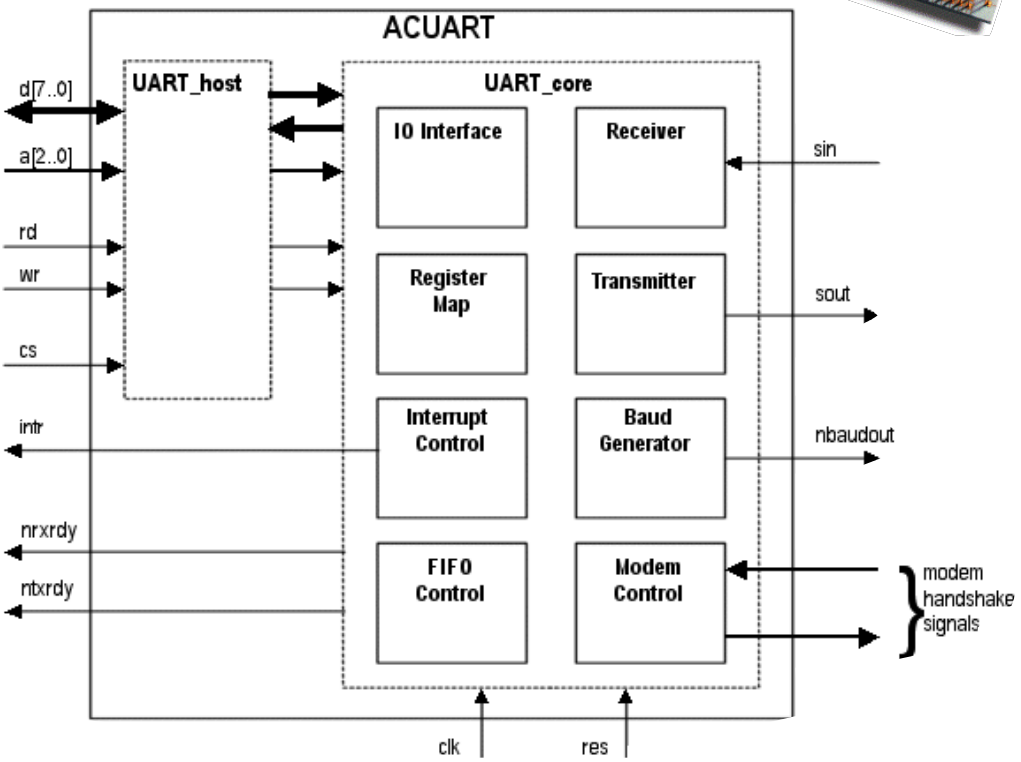
## BLOCK UART_HOST

Provides the interpretation between 16550 interface and UART_core interface - latches address and chip select signals, generates read enable and write enable signals synchronized with system clock, etc.

## BLOCK UART_CORE

The core of the ACUART. Transforms parallel data from the host to serial output and serial input to parallel data for the host. Controls modem handshake signals, generates the baud rate clock, indicates interrupts, DMA signals, etc.

## BLOCK DIAGRAM




Description of the blocks of UART_core:

| Block name | Description |
|---|---|
| IO Interface | Translates addresses to register select signals. Selects the register for reading |
| Register Map | Includes registers for setting serial communication parameters (Line Control Register), for reading status of the serial communication (Line Status Register) and the Scratch Register for user data storage. Controls ntxrdy and nrxrdy signals generation |
| Interrupt Control | Accepts interrupt source signals from other blocks. Masks interrupts using the Interrupt Enable Register. Prioritizes enabled interrupts. Generates the intr (interrupt) signal. Specifies the interrupt source in the Interrupt Identification Register |
| FIFO Control | Includes FIFOs for the Receiver and the Transmitter, the FIFO Control Register and the FIFO control logic. In the 16550 FIFO mode stores received characters and characters prepared for the transmission. Checks the trigger level for the Receiver FIFO. Counts the time-out for received data. Indicates the presence of character with error in the Receiver FIFO |
| Receiver | Receives data from the sin (serial input) signal. Serial input transforms to the parallel data. Detects transmission errors: break, frame, overrun and parity error. Includes the Receiver Holding Register and the Receiver control logic |
| Transmitter | Transmits data to the sout (serial output) signal. Parallel data transforms to the serial output. Includes the Transmitter Holding Register and the Transmitter control logic |
| Modem Control | Drives nrts, ndtr, nout1 and nout2 (modem handshake) output signals and monitors ncts, ndsr, ndcd and nri (modem handshake) input signals. Includes the Modem Control Register, the Modem Status Register and the Modem control logic |
| Baud Generator | Divides the clk (system clock) signal with divisor defined by the Divisor Latch Registers and generates clock signal for the Receiver and the Transmitter and the nbaudout signal with the same period |

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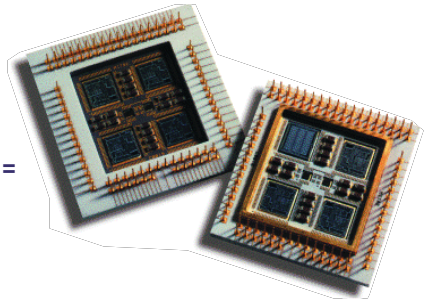
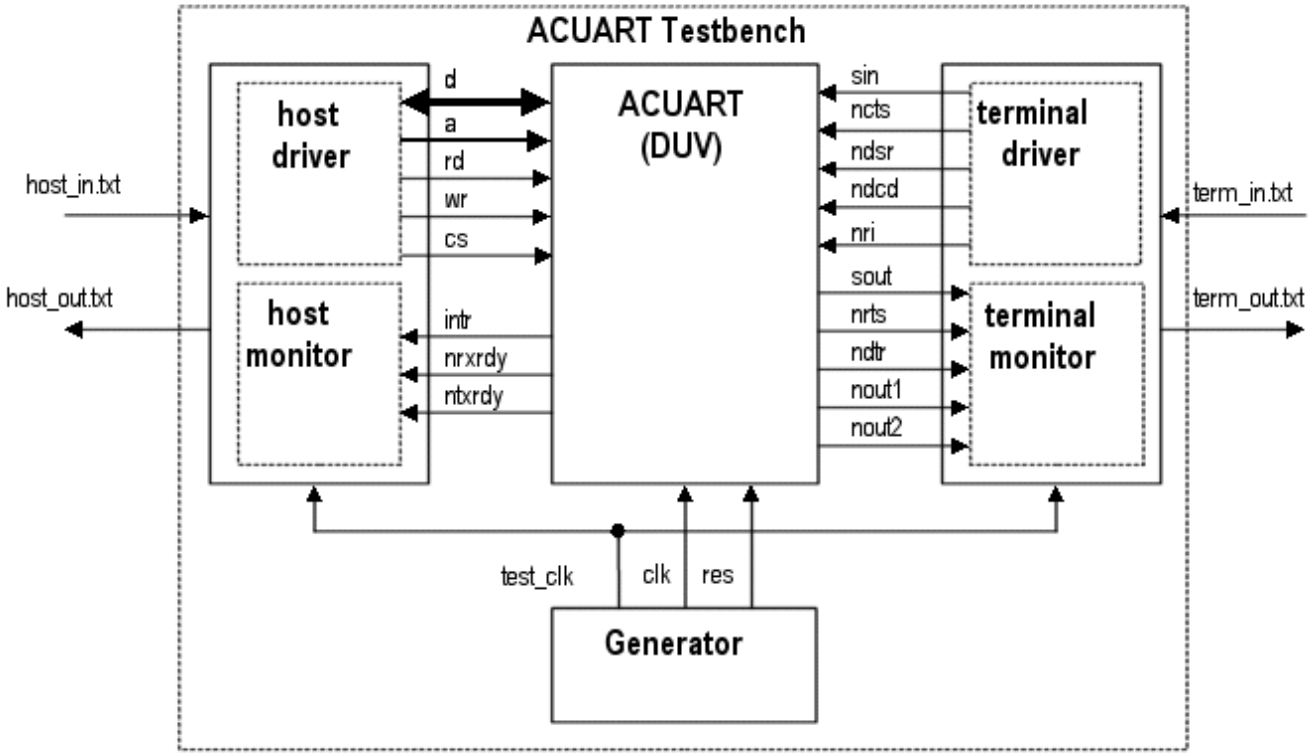


## ACUART REGISTERS

| Register name | Shortcut | Description |
|---|---|---|
| Receiver Buffer Register | RBR | Holds received character. |
| Transmitter Holding Register | THR | Holds character to be transmitted. |
| Interrupt Enable Register | IER | Masks interrupt sources. |
| Interrupt Identification Register | IIR | Identifies interrupt source, when intr (interrupt) signal is active. Indicates FIFO mode. |
| FIFO Control Register | FCR | Enables/disables the Receiver and the Transmitter FIFO. Resets the Receiver and the Transmitter FIFO (independently). Selects DMA mode and trigger level. |
| Line Control Register | LCR | Sets the serial communication parameters: number of data bits, length of stop bit, parity selection, set break etc. |
| MODEM Control Register | MCR | Drives modem handshake output signals, sets loopback mode. |
| Line Status Register | LSR | Indicates status of the serial communication. Includes Receiver ready, Trasmitter empty, Receiver break, frame, overrun and parity error bits. |
| MODEM Status Register | MSR | Indicates values and states of modem handshake input signals. |
| Scratch Register | SCR | Register for user data storage |
| Divisor Latch(lower byte) | DLL | Defines divisor for the Baud Generator |
| Divisor Latch(higher byte) | DLM | Defines divisor for the Baud Generator |

## VERIFICATION METHODS

The ACUART core was verified by digital simulation at both RTL and gate level.
For the host signals driving and monitoring the host driver and monitor are utilized. The host driver reads the host command file host_in.txt and controls host input signals. On the other hand the monitor scans host output signals and writes results to the host_out.txt log file.
The terminal driver/monitor handles the serial data and modem handshake signals in the same way.



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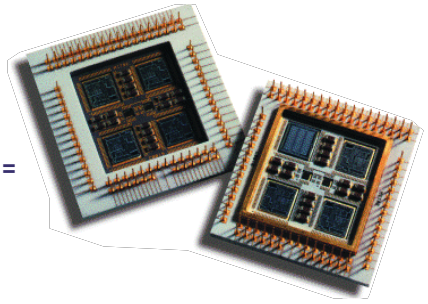
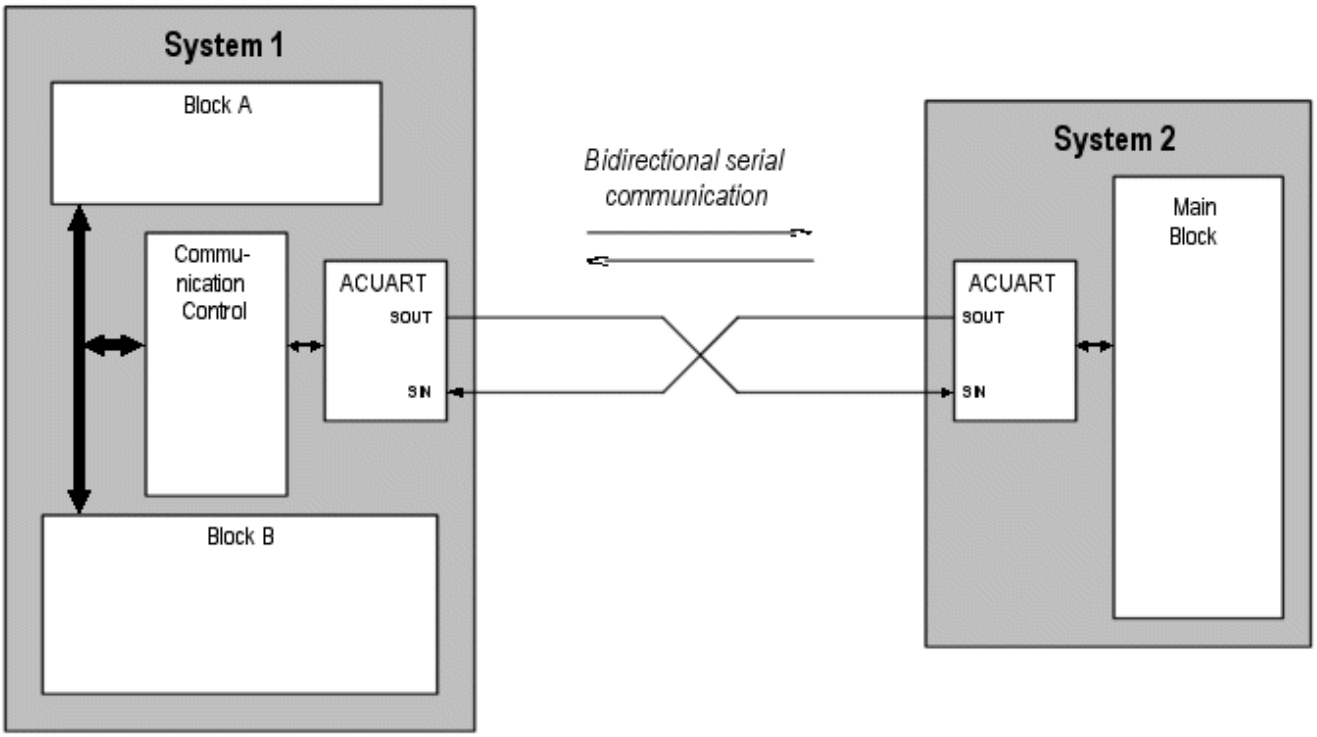


## TYPICAL APPLICATIONS

The ACUART can be used in any application, where the bidirectional communication is required. It needs only three lines to realize the communication. The serial line errors protection and the transmission errors detection increases the communication reliability. The FIFOs and prioritized interrupts minimize the system time spent to serve the communication.




The ACUART can be used as an interface between systems with any architectures. The system uses the host interface of ACUART to control the communication.