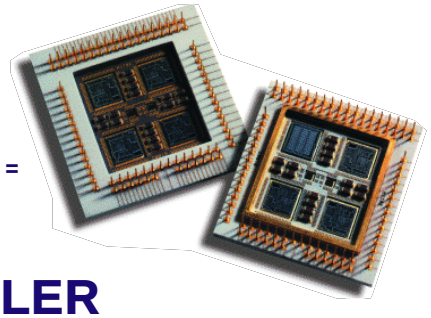
ASICentrum A COMPANY OF THE SWATCH GROUP
Novodvorska 994, 142 21 Praha 4, Czech Republic
Tel. (+420 2) 4404 3478, Fax: (+420 2) 4149 2691, E-mail: info@asicentrum.cz



ACPIC IP CORE
PIC16C55 – 8BIT MICROCONTROLLER

BASIC PARAMETERS

Equivalent to PIC16C55 Microchip device

- Up to 512 instructions in ROM
- 12-bit wide instructions
- 8-bit wide data path
- 8 special function registers (SFR)
- 24 general purpose registers (GPR)
- two-level deep hardware stack
- direct, indirect and relative addressing modes for data and instructions
- synchronous watchdog reset via WDT_IN pad
- 20 I/O pins

Enhancements and differences

- 8-bit programmable real time clock/counter with 8-bit programmable prescaler
- modularity and configurability of core components
  - number of ports and clock/counter registers definition
  - width of ports adjustment
  - depth of stack adjustment
  - new instructions addition
- easy expandable with non-standard peripheral components
- system clock frequency up to 20MHz (technology dependent)
- only 32 single word instructions (sleep is not implemented)

FEATURES

- fully synthesisable VHDL macro
- technological independence
- 5500 gates complexity

DELIVERABLES

- Design file formats
  - RTL VHDL synthesisable code
  - Netlist
- Technical documentation
  - data sheet
  - implementation guide
- Verification tools
  - Testbench
- Constraints files
- Maintenance

REGISTER FILE MAP

ADDRESS	NAME	DESCRIPTION
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/Watchdog prescaler
00H	INDF	Uses contents of FSR register to address data memory
01H	TMR0	8-bit real-time clock/counter
02H	PCL	Low order 8bits of PC
03H	STATUS	Status register
04H	FSR	Indirect data memory address pointer
05H	PORTA	4-bit I/O port
06H	PORTB	8-bit I/O port
07H	PORTC	8-bit I/O port
08H-1FH	GPRs	General Purpose Registers

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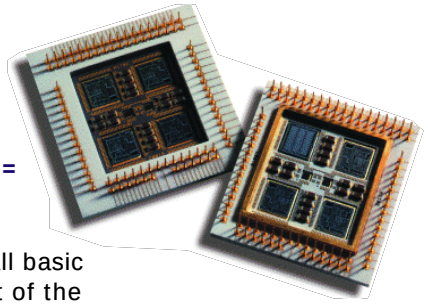
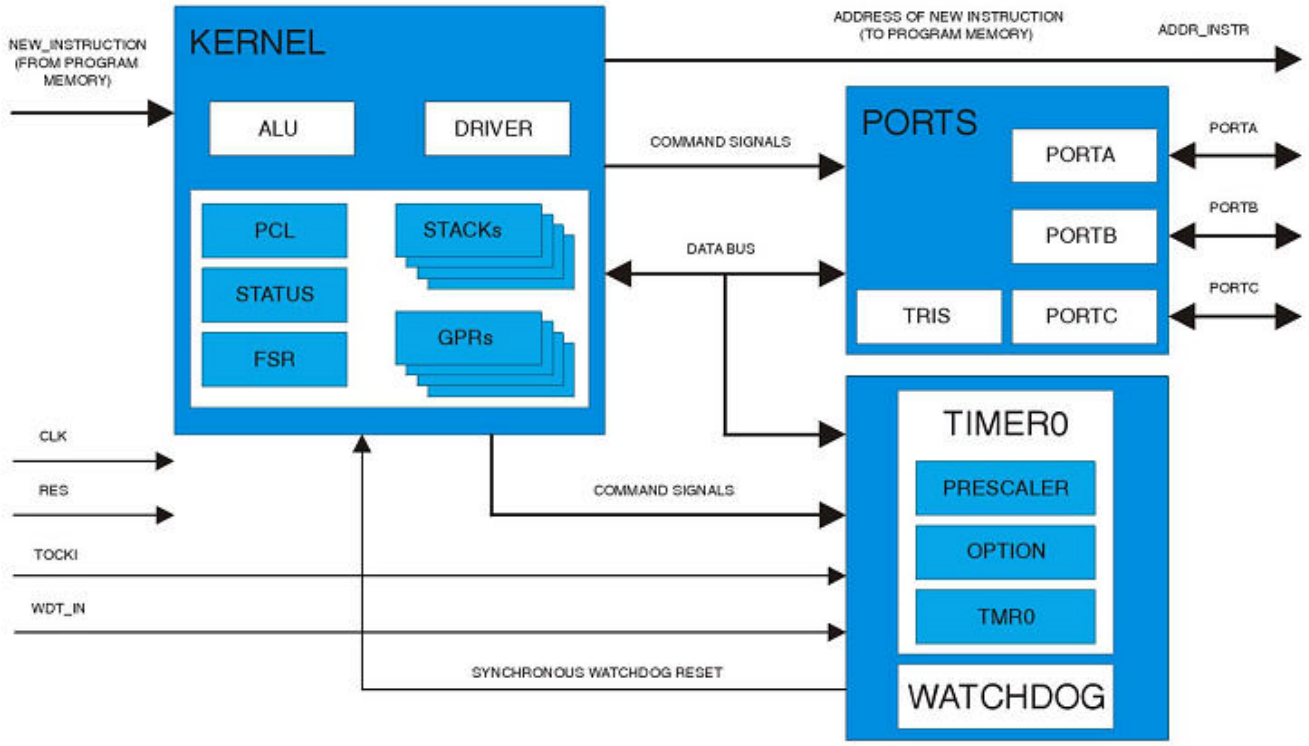


BLOCK DIAGRAM

The ACPIC core is partitioned into modules. ACPIC kernel module contains all basic elements such as ALU, instruction decoder, registers, stacks and so on. Rest of the elements (ports, timer module, watchdog) are connected with the kernel via internal data bus and other control signals.



DIFFERENCES BETWEEN ORIGINAL PIC AND ACPIC

Diff. Number	Name	Type of difference	Standard PIC	ACPIC
1	Program memory	Design Structure	Standard PIC includes Program memory	ACPIC requires external Program memory (core is merged with Program memory during synthesis process)
2	Clock signals	Timing	Standard PIC uses 4 clock domains	ACPIC uses single clock signal and 4 clock enable signals
3	Watchdog	Design Structure	Standard PIC uses internal oscillator for Watchdog	Watchdog clock signal can be connected to WDT_IN pin
4	Enhanced Timer0	Behaviour	Incrementation of Timer0 is inhibited for 2 clock cycles after it was written a value	Incrementation of Timer0 is inhibited for 1 instruction cycle after it was written a value
5	Write to PC	Behaviour	When the PC is modified as a result of ALU operation, next instruction is forced to NOP	When the PC is modified as a result of ALU operation, next instruction is executed
6	Sleep instruction	Instruction set	SLEEP instruction enforces low power mode	SLEEP instruction is not implemented

When some of this differences make a problem for your application, please contact ASICentrum for available solutions.

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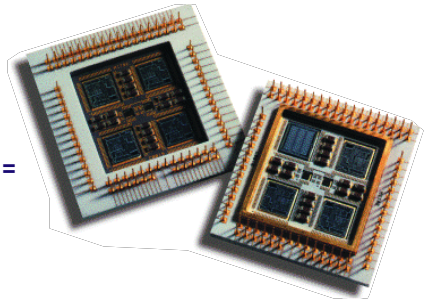


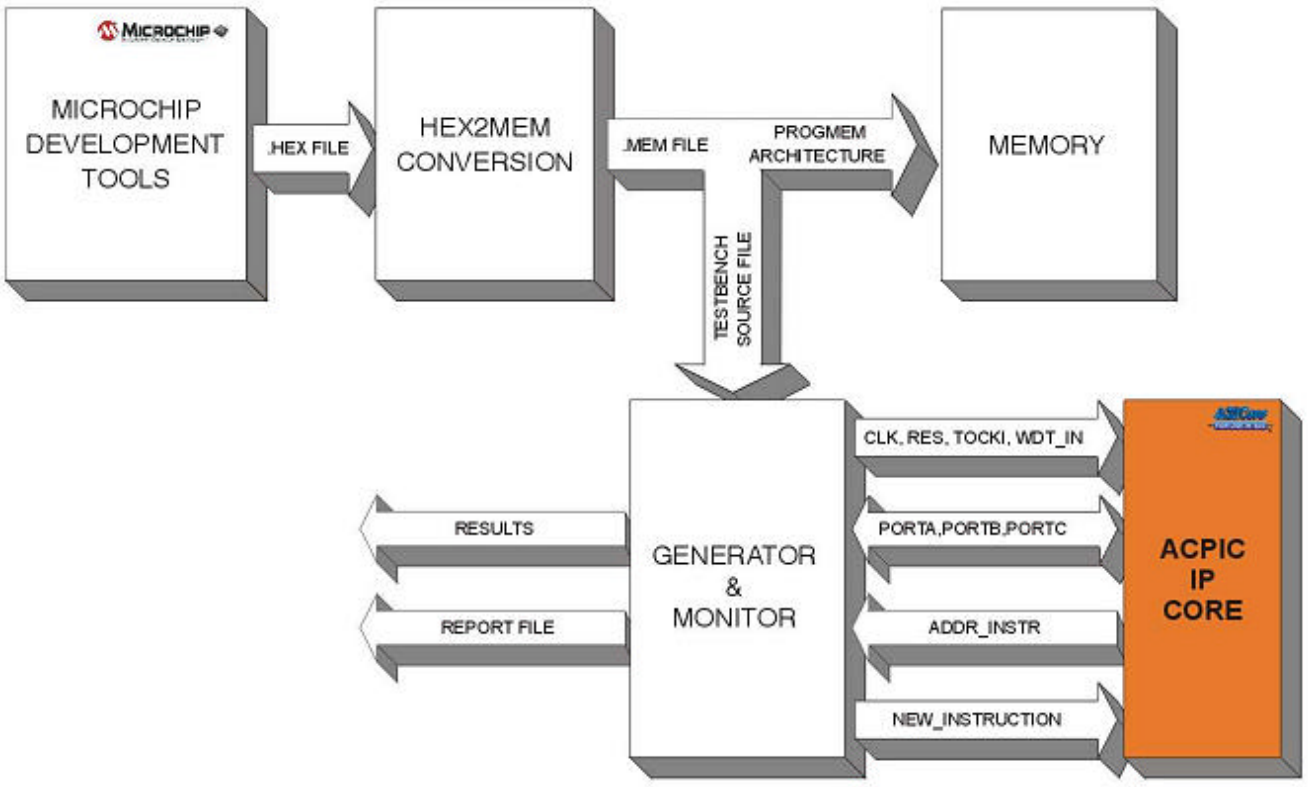
CONFIGURABILITY OPTIONS OF ACPIC CORE

Name	Description	Level of complexity
Width of ports	Width of ports can be changed using generic parameters	Small
Adding of ports	Adding of ports is possible, but it requires the change of address map and address decoders	Small
Changing the number of GPR	Number of registers can be changed, address map must be redefined	Small
Changing the depth of hardware Stack	It is possible to support multiple levels of call nesting	Small
Migration to other PIC16C5X	This can be done relatively easily by changing the address map and decoding	Easy / medium
Adding of non standard PIC peripherals	Adding of another peripheral requires the definition of interface and address location	Medium - depends on the type of peripheral
Changing the width of data	Internal data bus and ALU width can be changed. Some bit-level instruction may not be supported	Medium / high
Adding of customer specific instructions	It is possible, to add customer instruction, but they must conform general ACPIC timing	Medium / high

VERIFICATION METHODS

Hardware proven
Xilinx FPGA prototype was created for the real time testing of the core.

Simulation
The core was tested on RTL and gate level using testbench developed by ASICentrum.



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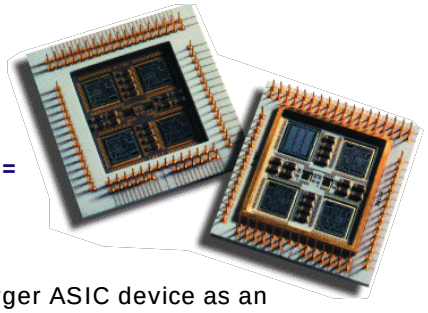
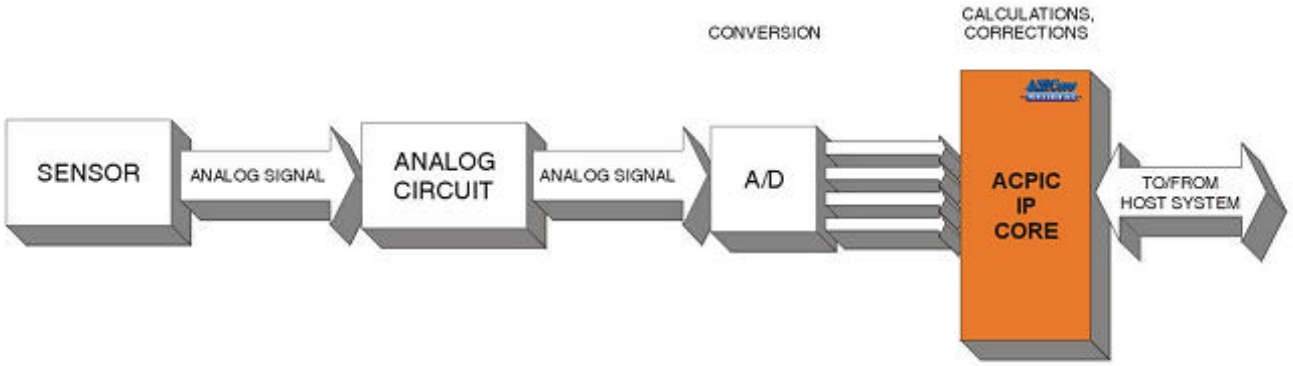


TYPICAL APPLICATIONS

ACPIC core is very flexible macro of microcontroller which can be used in larger ASIC device as an microprocessor. Typical applications include :

- DSP post processing (evaluation of filter results, ...)
- simple USB device controller (together with ACUSB)
- migration from single-board to single-chip solution

Smart sensor



DSP post processing (evaluation of filter results)