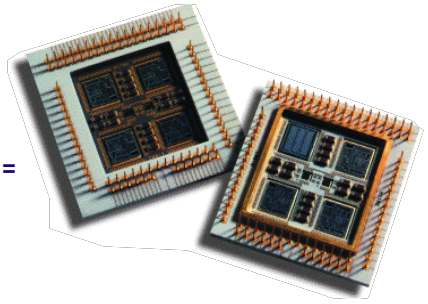
ASICentrum A COMPANY OF THE SWATCH GROUP
Novodvorska 994, 142 21 Praha 4, Czech Republic
Tel. (+420 2) 4404 3478, Fax: (+420 2) 4149 2691, E-mail: info@asicentrum.cz



ACPCI IP CORE - PERIPHERAL COMPONENT INTERCONNECT BUS

BASIC PARAMETERS

Fully compliant to PCI V2.2 specification

- master (initiator/target) configuration
- bus parking and zero wait – state burst operations
- 2 base address registers for application memory or I/O ports
- control signal register for PCI bus monitoring
- transfer latency controlled by application
- 8-bit preset latency timer with automatic synchronous set
- 32-bit architecture
- 0 – 33 MHz system clock

Enhancements and differences

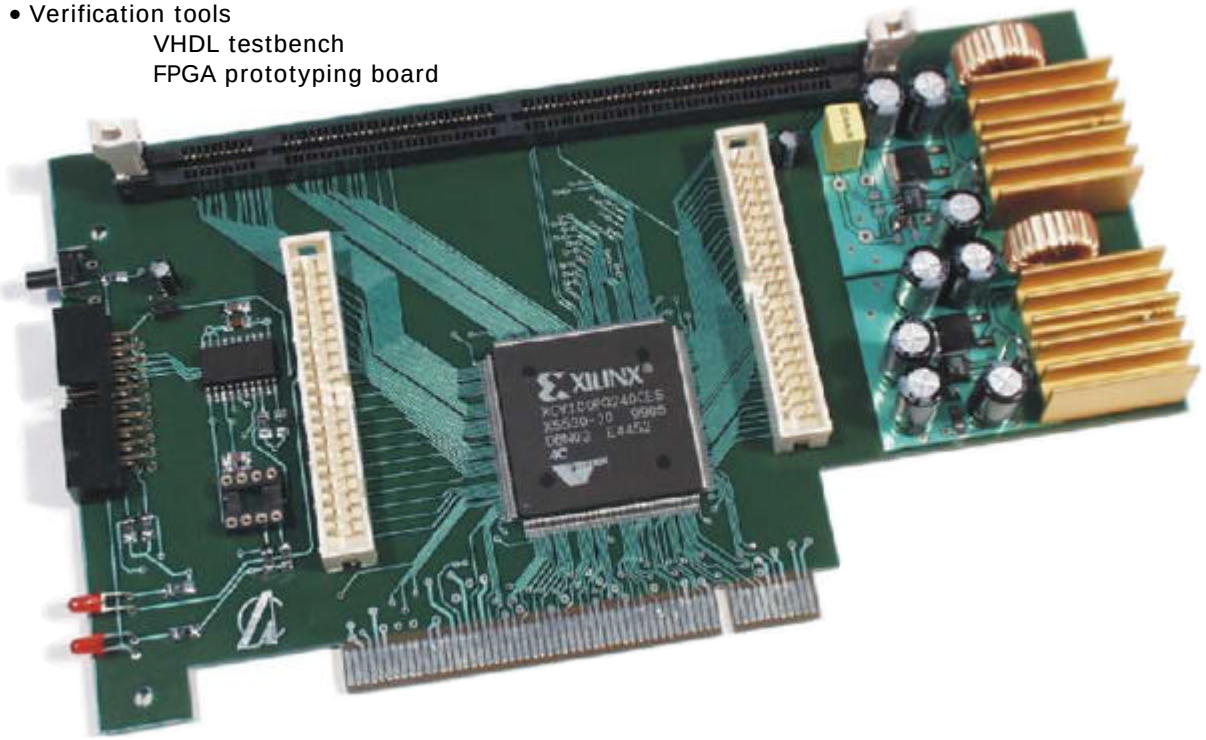
- locked operation supported
- 1 interrupt signal

FEATURES

- completely synchronous design
- four-layer hierarchical VHDL structure
- technological independence
- fully verified design

DELIVERABLES

- Design file formats
  - RTL VHDL synthesisable code
  - Netlist
- Technical documentation
  - Data sheet
  - Implementation guide
- Constraints files
- Maintenance
- Verification tools
  - VHDL testbench
  - FPGA prototyping board



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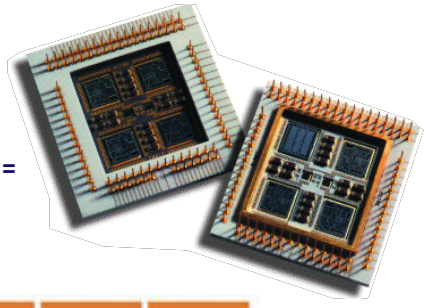

BUS COMMANDS

CBE (3:0)	Command	PCI Master	PCI Slave
0000	Interrupt Acknowledge	Yes	Ignore
0001	Special Cycle	Yes	Ignore
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	Ignore	Ignore
1001	Reserved	Ignore	Ignore
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	No	Ignore
1110	Memory Read Line	Yes	Yes
1111	Memory Write and Invalidate	Yes	Yes

CONFIGURATION SPACE HEADER

31 – 24	23 – 16	15 – 8	7 – 0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Registers	BAR 0			10h
	BAR 1			14h
	BAR 2			18h
	BAR 3			1Ch
	BAR 4			20h
	BAR 5			24h
Cardbus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			*Cap Pointer*	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved				40h-FFh

NOT IMPLEMENTED IN ACPCI IP CORE

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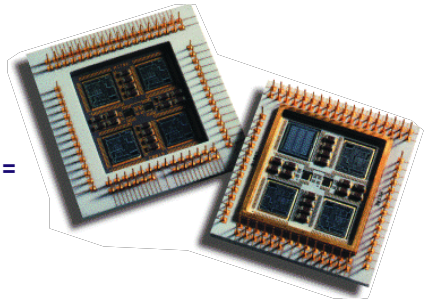

INTERFACE SIGNALS OVERVIEW

Signal	Initiator	Target	Functional Description
PCI bus interface signals			
AD[31:0]	I/O	I/O	Time multiplexed PCI address/data bus
CBE[3:0]	I/O	I	PCI command/byte enable
PAR	I/O	I/O	Even parity for AD and CBE (one clock cycle delayed)
FRAME#	I/O	I	Indicate duration of the PCI transaction
TRDY#	I/O	O	Indicate that the Target is ready to complete the current data phase
IRDY#	I/O	I	Indicate that the Initiator is ready to complete the current data phase
STOP#	I/O	O	Indicate that the Target want to stop the current PCI transaction
DEVSEL#	I/O	O	Indicate that the Target device was selected
IDSEL	I	I	Selects current device as a target for configuration transaction
PERR#	I/O	O	PCI Parity Error
SERR#	I/OD	OD	PCI System Error
REQ#	O	N/A	Initiator request for PCI ownership
GNT#	I	N/A	Arbiter grants the PCI ownership
LOCK#	I	I	Target lock signal (supported in Target mode only)
INTA#	O	O	PCI Interrupt Request
CLK	I	I	0 - 33 MHz PCI system clock
RST#	I	I	PCI system reset
User Interface signals			
CFG[255:0]	I	I	Core configuration bus - for core customisation
FRAMEQ_N	O	O	Registered version of signal FRAME#
IRDYQ_N	O	O	Registered version of signal IRDY#
TRDYQ_N	O	O	Registered version of signal TRDY#
STOPQ_N	O	O	Registered version of signal STOP#
DEVSELQ_N	O	O	Registered version of signal DEVSEL#
ADDR[31:0]	O	O	Target address of PCI transaction
ADIO[31:0]	I/O	I/O	Bidirectional internal address/data bus
T_CBE[3:0]	O	O	Indicates command / byte enable for current transfer
ADDR_VLD	O	O	Indicates that ADIO contains the valid address during Target data transaction
CNFG_VLD	O	O	Indicates that ADIO contains the valid address during configuration transaction
T_DATA_VLD	O	O	Target data are valid on ADIO
T_WRDN	O	O	Indicates PCI transaction direction
PCI_CMD[15:0]	O	O	Indicates the type of the current PCI transaction
BASE_HIT[7:0]	O	O	Indicates that address has matched some base address register
CFG_HIT	O	O	Indicates that the device was selected as a target for configuration transaction
C_READY	I	I	Indicates that the device is ready to transfer the data from the user configuration space
C_TERM	I	I	Indicates that the device wants to stop the configuration transaction to the user configuration space
T_SRC_EN	O	O	Increments the address counters during Target burst transactions
T_READY	I	I	Indicates that the device is ready to transfer the data for Memory / I/O transactions
T_TERM	I	I	Indicates that the device wants to stop the current Memory/ I/O transactions
T_ABORT	I	I	Indicates that the device wants to abort the current Memory / I/O transaction
REQUEST	I	N/A	Device request for the bus ownership
I_CBE[3:0]	I	N/A	Command / byte-enables for Initiator transaction
I_WRDN	I	N/A	Initiator transaction direction
COMPLETE	I	N/A	Initiator wants to complete the current transaction
I_READY	I	N/A	Initiator is ready to transfer the data in the current data phase
I_SRC_EN	O	N/A	Initiator source data enable
I_DATA_VLD	O	N/A	Initiator data valid
TIME_OUT	O	N/A	Latency timer timeout
KEEPOUT	I	I	Isolates internal ADIO bus from the PCI transactions
I_DATA	O	N/A	Initiator data phase
DR_BUS	O	N/A	Device is driving the PCI bus
I_ADDR_N	O	N/A	Address phase of initiator transaction
I_IDLE	O	N/A	Initiator FSM is in the Idle state
IDLE	O	O	Target FSM is in the Idle state
B_BUSY	O	O	Target FSM is in Busy state
T_DATA	O	O	Target FSM is in Data state
BACKOFF	O	O	Target FSM is waiting for the transaction to complete
PERRQ_N	O	O	Registered version of PERR#
SERRQ_N	O	O	Registered version of SERR#
CSR[39:0]	O	O	Extended command / status
SUB_DATA[31:0]	I	I	Subsystem ID, Vendor ID
INTR_N	I	I	Interrupt request signal

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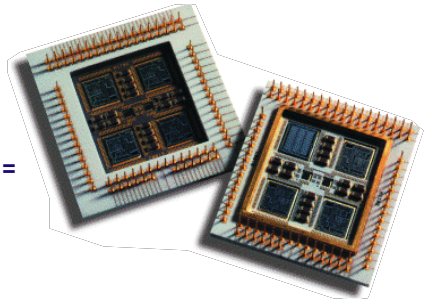

TYPICAL APPLICATIONS

Add-in boards

- video adapters
- LAN adapters
- data acquisition boards
- graphic cards

Embedded applications

- networking
- telecommunication
- industrial systems

INTERNAL STRUCTURE AND APPLICATION EXAMPLE