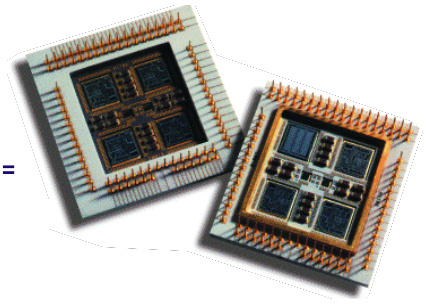
ASICentrum® A COMPANY OF THE SWATCH GROUP
Novodvorska 994, 142 21 Praha 4, Czech Republic
Tel. (+420 2) 4404 3478, Fax: (+420 2) 4149 2691, E-mail: info@asicentrum.cz



ACIIR IP CORE
IIR FILTERS

BASIC PARAMETERS

- Configurable fixed point IIR filters
- DSP processor architecture
- 2’s complement arithmetic
- Parametrisable data and coefficient widths
- Configurable precision and output scale ability
- Filter algorithm specified by program in internal ROM (RAM)
- Expandable instruction set of 24 instructions
- Coefficients stored in internal ROM (RAM)

Optional enhancements

- Interface to PCM telecom ADC (a-law compression, 2’s complement, 8 bits)
- Interface to coprocessor - post processing - (ACPIC core can be used for post processing)
- Interface to host CPU - mode control

FEATURES

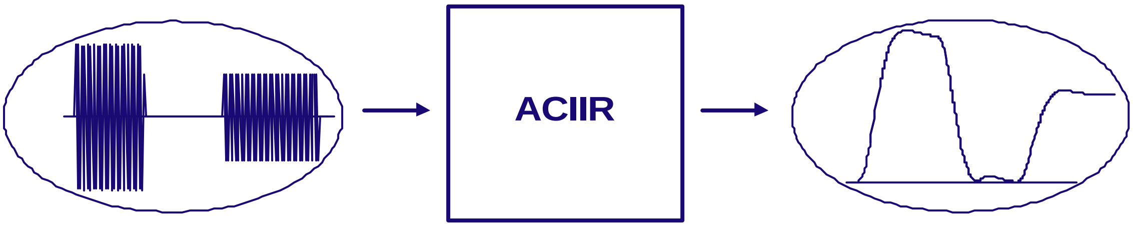
Fully synchronous synthesisable RTL VHDL macro
Technological independenence
Fully verified according compliance checklist
Complexity aprox. 20K gates

DELIVERABLES

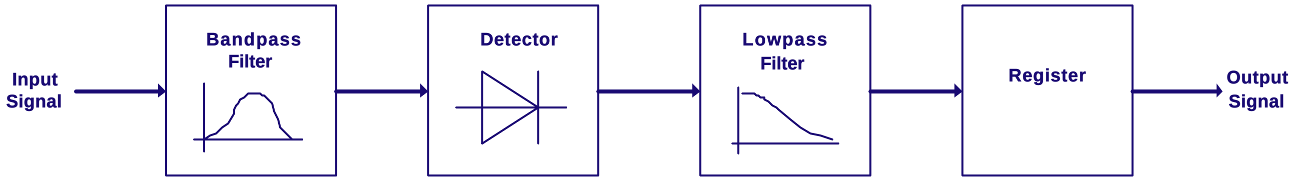
- Design file formats
  - RTL VHDL synthesisable code
  - Netlist
- Technical documentation
  - Data sheet
  - Implementation guide
- Verification tools
  - Testbench
  - FPGA prototyping board
  - Silicon
- Constraints files
- Maintenance

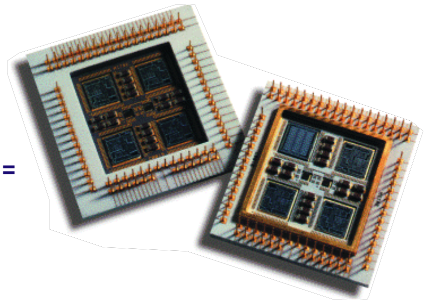
ACIIR DESCRIPTION

ACIIR is a simple digital signal processor in function of programmable filter. All functions are implemented digitally inside the core. The core was developed in VHDL language, using only standard and IEEE packages.



BLOCK SCHEMATIC





FILTER REALIZATION

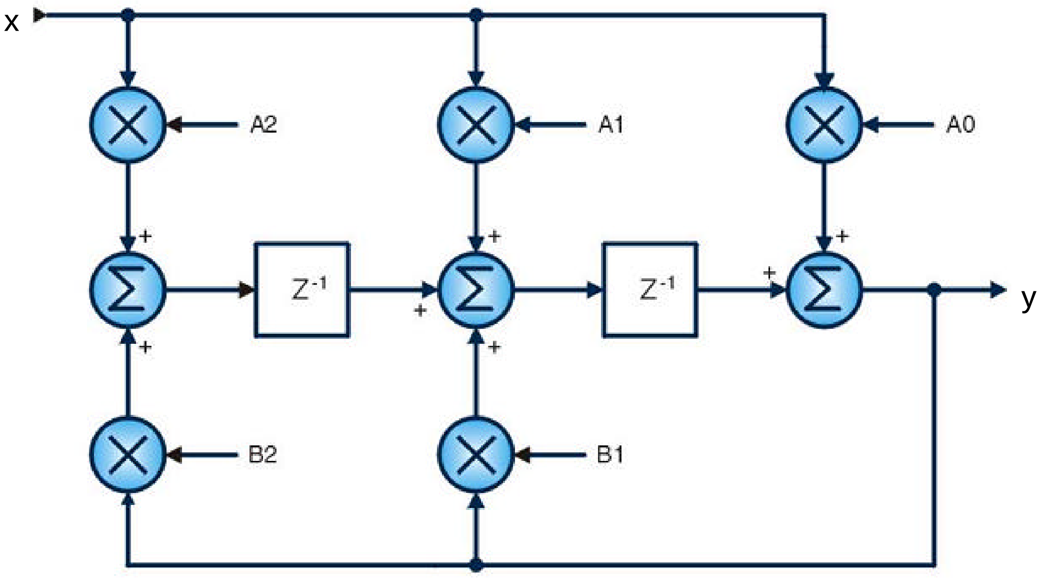
IIR digital filters are characterized by the following recursive equation:

$$y(n) = \sum_{i=0}^{N-1} a(i)\,x(n-i) - \sum_{i=1}^{N-1} b(i)\,y(n-i)$$

where a(i) and b(i) are the coefficients of the filter, and x(n) and y(n) are the input and output to the filter.

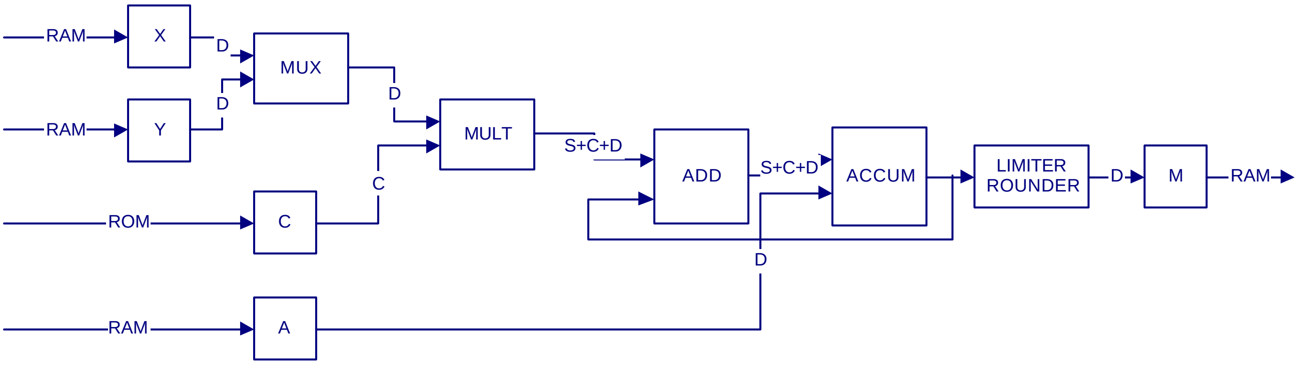
ACIIR filter is realized by means of biquads, which make use of algorithm balanced pole zero. The detector is realized with function absolute value.

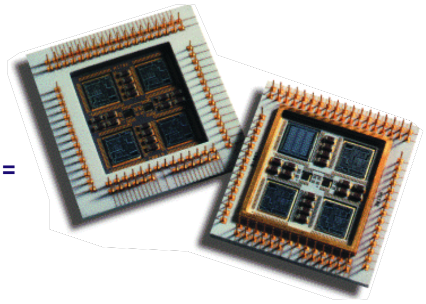
BLOCK DIAGRAM REPRESENTATION OF BIQUAD



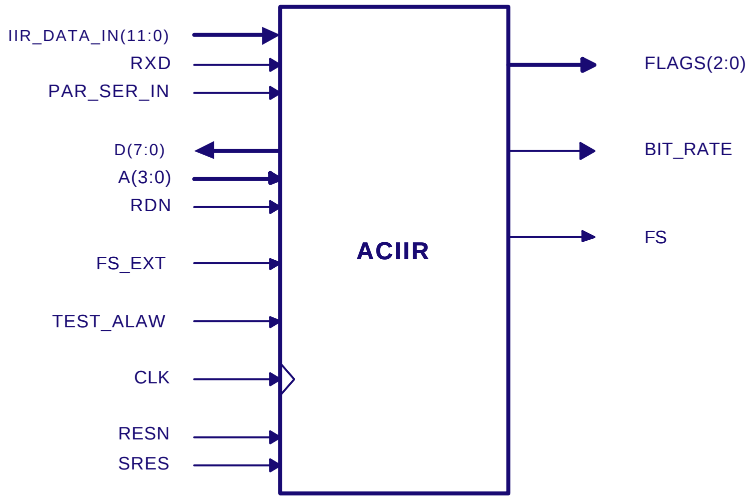
Whole operations with data (transfer A/D, multiplication, accumulation, absolute value, comparison) pursue by means of executive unit ALU and Detector in block EXU.

BLOCK SCHEMATIC FOR ALU

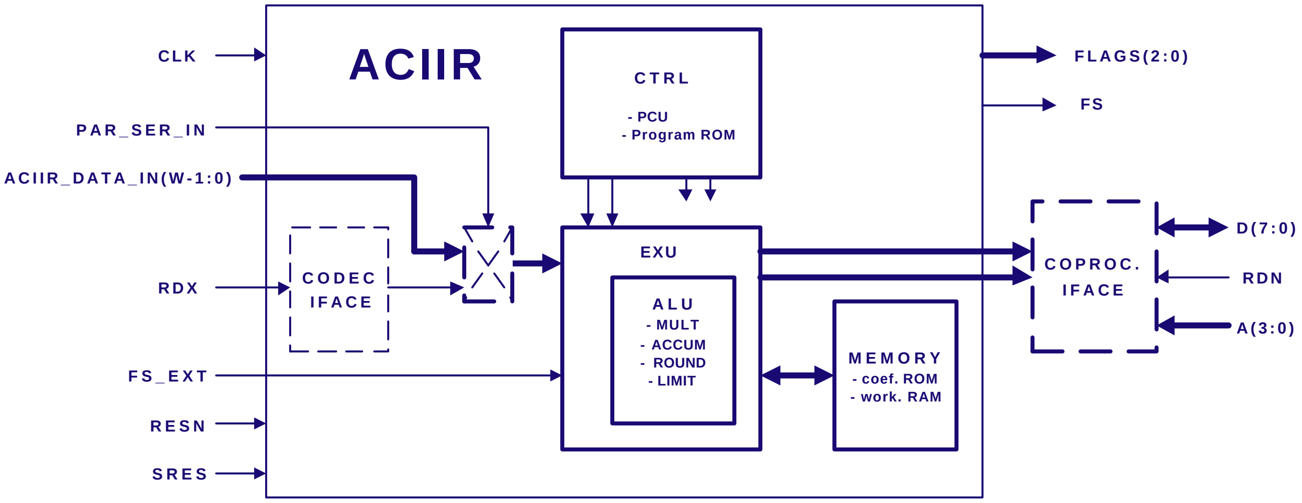




ACIIR INTERFACE



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

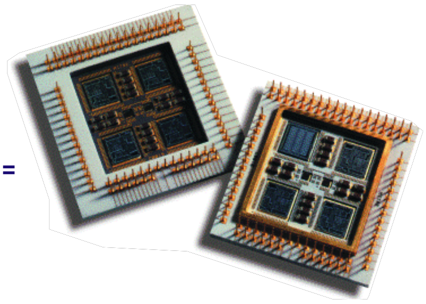
Data are processed in Execution Unit (EXU). It consists from Arithmetic and Logical Unit (ALU) and set of registers. ALU includes 2’s complement serial multiplier with Booth encoding, accumulator and rounder/ limiter block. Intermediate results are stored in Memory - working RAM block. Coefficients are read from Memory - coefficient ROM block. Memory and EXU are connected by internal bus.

Results of computation are presented using Coprocessor Interface to an external coprocessor (ACPIC core can be used for post processing).

Control (CTRL) block includes Program ROM with filtering algorithm and Program Control Unit (PCU) which interprets instructions and generates control signals for data processing blocks.

Flexibility of program control allows to implement both filters on received signal and generators of transmitted signal using the same EXU if demanded. The only difference is in control program. Mode CTRL block can select one of the programs for execution. Mode of operation is controlled by external processor via Host CPU Interface block.

Received incoming data (for filtering) and outgoing transmitted data (after generation) can be converted using Codec IFACE to standard serial data stream.



ACIIR PINOUT

Port name	Direction	Description
CLK	Input	System clock 18.432MHz
RESN	Input	Asynchronous global reset, active Low
RXD	Input	Serial input data, A-law format
IIR_DATA_IN(width_iir_in-1 : 0)	Input	Parallel input data
PAR_SER_IN	Input	Choose parallel or serial input data for processing
A(3:0)	Input	Address bus for read from Coprocessor
RDN	Input	Read signal, active Low
SRES	Input	Synchronous reset, active High
TEST_ALAW	Input	Control signal, connect data to output
FS_EXT	Input	8kHz frame for data
BIT_RATE	Output	Clock for Codec, 2.048Mhz
FS	Output	8kHz frame for Codec
FLAGS(2:0)	Output	Flags bus: rounding UP, limited to max positive ($7FFFF), limited to max negative($80000)
D(7:0)	Output	Coprocessor data bus

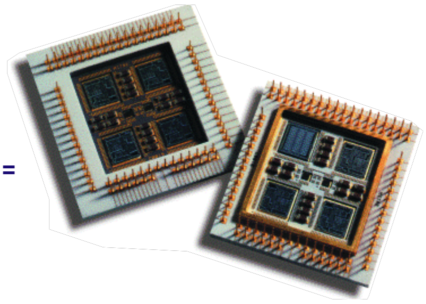
CORE PARAMETERISATION

ACIIR is flexible and allows easy modification according customer's need. This modification is provided by ASICentrum and may include :

- Filter algorithm specification using ACIIR instruction set
- Data-word width
- Coefficient precision
- ALU precision
- Rounding/limiting behaviour
- RAM/ROM size
- Custom instructions may be included

The list of generic parameters :

Generic	Type	Description
width	Integer	GDB width
widthC	Integer	ALU coef. bus width
width2	Integer	direct input ACCUM width
width_iir_in	Integer	parallel data input width
wext	Integer	sign extension width
ramd_depth	Integer	
romc_depth	Integer	
ci_width	Integer	coprocessor data width



TECHNOLOGY SPECIFIC ISSUES

Core is implemented as fully synchronous synthesizable RTL VHDL code. For internal RAM, synchronous model was used to reflect primary FAGAN RAM implementation. This type of memory may not be directly supported by customer technology or synthesis tool and specific solution may be needed.

FPGA IMPLEMENTATION OVERVIEW

GDB width (bits)	Device	Max. Frequency [MHz]	Utilization	Equivalent Gates
17	XCV50-4	31,242	93% Slices	19 871
20	XCV50-4	29.428	96% Slices	21 983
22	XCV50-4	27.628	94% Slices	22 830
22	XC4028XL-09	18.691	73% CLB	17 374
22	XCS40-3	12.644	95% CLB	17 367

VERIFICATION METHODS

ACIIR core has been tested using functional and post-layout timing VHDL simulation (after FPGA implementation).
Finally core was silicon proven via FPGA conversion to Orbit GA.

TYPICAL APPLICATIONS

- DTMF receiver
- PCM signal receiver