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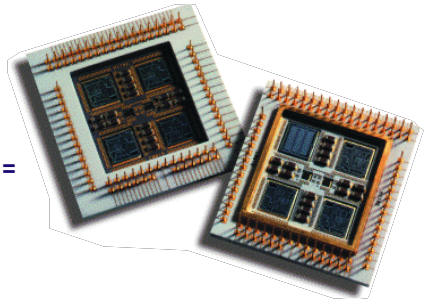


# ACDPLL IP CORE
# DIGITAL PHASE LOCKED LOOP

## BASIC PARAMETERS

- Fully synthesizable technology independent HDL macro
- Fully digital design with no external components
- Frequency range from 0 MHz
- Different phase detectors
- Programmable loop filter
- Accuracy is not affected by temperature and supply voltage variations
- Adaptable to user requirements

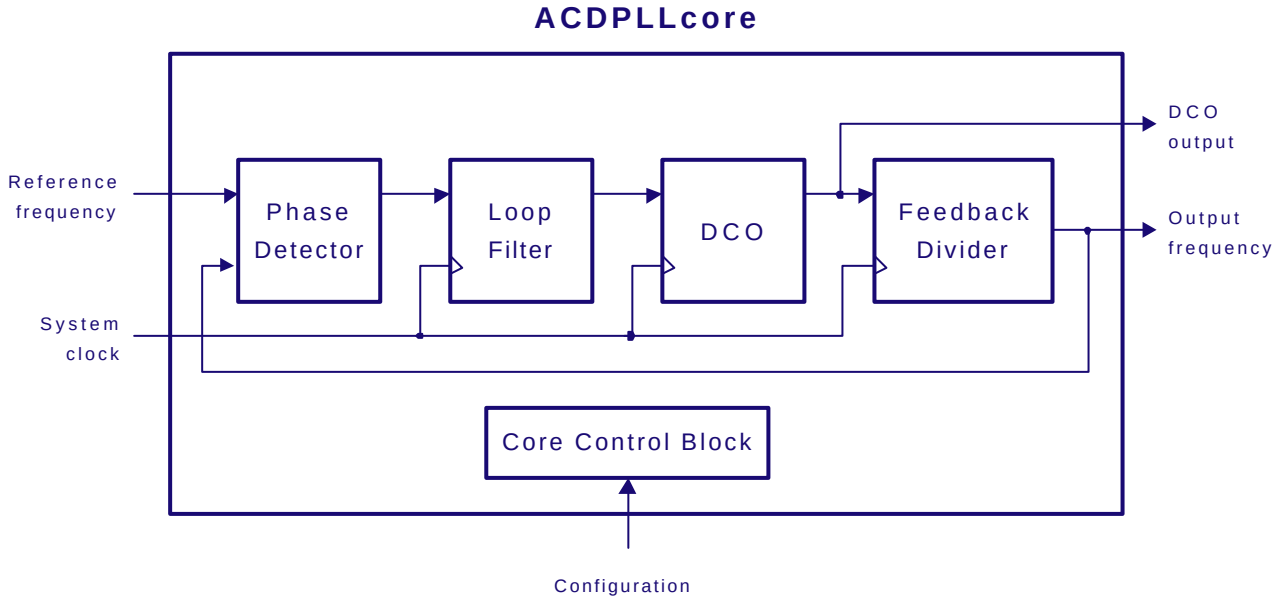
## FEATURES

Synchronous design (except the phase detector)
Technological independenence
Approximate gate count : 1500

## DELIVERABLES

- Design files
  - RTL VHDL synthesizable code
  - Netlist
- Technical documentation
  - Data sheet
  - Implementation guide
- Verification tools
  - VHDL testbench
  - FPGA prototyping board
- Constraints files
- Maintenance

## BLOCK DIAGRAM



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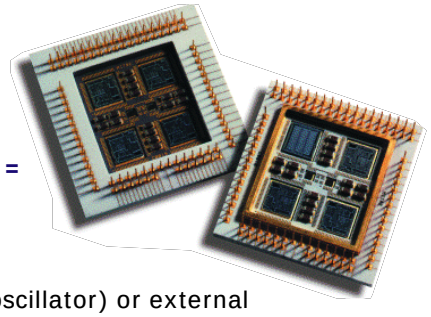

## FUNCTIONAL DESCRIPTION

Main advantage of the ACDPLL is that no external VCO (Voltage controlled oscillator) or external components are needed. All blocks are implemented fully digitally. Block diagram describes architecture of the ACDPLL and represents structure of the first-order PLL.

**Phase Detector**
compares phase difference between synthesized output frequency and reference input. Commonly used XOR gate or edge sensitive phase detector can be selected.

**Loop Filter**
converts the phase difference from the phase detector to the frequency deviation. It is implemented as a first order filter and generates signals to control the DCO.

**DCO (Digitally Controlled Oscillator)**
Generated output frequency is controlled by the loop filter output. If no frequency correction is needed, output frequency is equal with the DPLL central frequency.

**Feedback Divider**
divides the DCO output frequency to achieve the same frequency as the reference input.

**Core Control Block**
sets up the ACDPLL block parameters, phase detector type, loop filter constant and feed back divider ratio. Also phase locking can be disabled.

## PINOUT

| Port name | Direction | Description |
|---|---|---|
| **Hardware configurable version** | | |
| clk | input | System clock input |
| res | input | Asynchronous system reset, active high |
| fref | input | Reference frequency input |
| pll_en | input | Enable phase locking, if not active center frequency is generated |
| pd_type (1:0) | input | Phase detector type selection |
| fout | output | Output after the feedback divider |
| fdco | output | DCO output |
| lf_const (3:0) | input | Loop Filter constant selection |
| fb_div (fb_w_g:0) | input | Feedback divider ratio |
| **Generics** | | |
| fb_w_g | integer | Feed-back counter width |
| **Synthesis configurable version** | | |
| clk | input | System clock input |
| res | input | Asynchronous system reset, active high |
| fref | input | Reference frequency input |
| pll_en | input | Enable phase locking, if not active generates center frequency |
| pd_type (1:0) | input | Phase detector selection |
| fout | output | Output after the feedback divider |
| fdco | output | DCO output |
| **Generics** | | |
| lf_const_g | integer | Loop filter constant selection |
| fb_w_g | integer | Feed-back counter width |
| fb_div_g | integer | Feed-back division ratio |

The hardware configurable version of the ACDPLL offers changing of parameters in the applications, these parameters are ACDPLL inputs. It naturally consumes more gates than the synthesis version.
On the other hand, the synthesis configurable version offers parameters setting as a HDL generic and cannot be changed during the circuit operation. This can be useful when the user application doesn't require to adapt core parameters.

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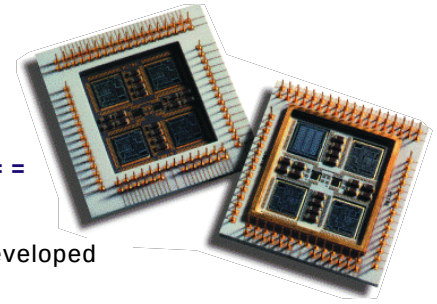
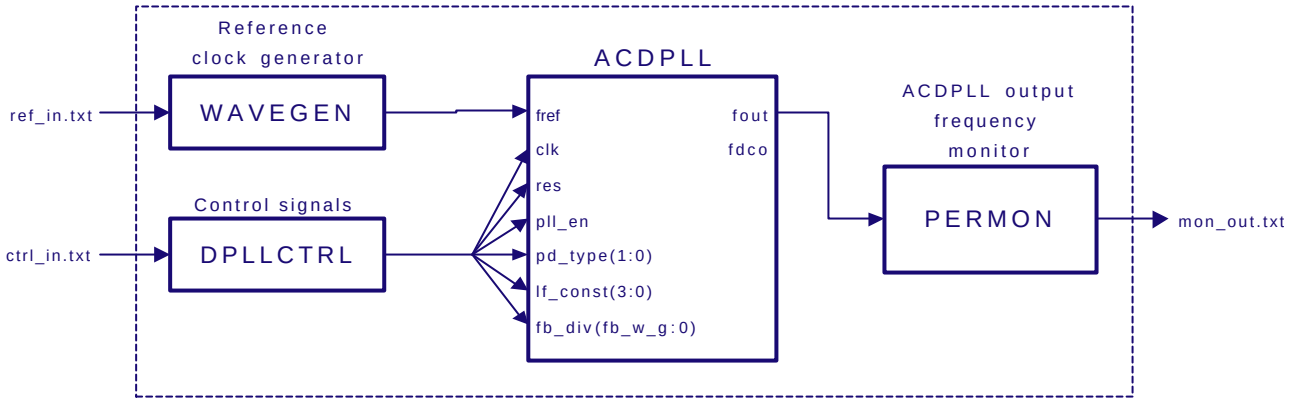


## VERIFICATION METHODS

ACDPLL has been synthesized in Xilinx FPGA and tested in ASICentrum's developed test board.

Simulation (testbench developed by ASICentrum)




Silicon proven in the ASIC application

- ISDN terminal adapter circuit
- 0,5µm/3,3-5V gate array CMOS technology

## APPLICATIONS

The phase locked loop (ACDPLL IP CORE) has a wide usage in many applications especially in telecommunications. The main application of ACDPLL is to slave a local oscillator to a remote reference clock source, but it can be used for other application, e.g. as a FSK decoder and other.

## QUESTIONNAIRE

DPLL parameters setting and implementation of some blocks depends on user application, therefore for our consideration is necessary to determine basic parameters of your application.

| Parameter | Value | Unit | Tolerance |
|---|---|---|---|
| Available system clock | | | |
| Reference frequency range | | | |
| Reference frequency width ratio | | % | |
| DCO center frequency | | | |
| DCO center frequency range | | | |
| Output frequency jitter amplitude | | | |