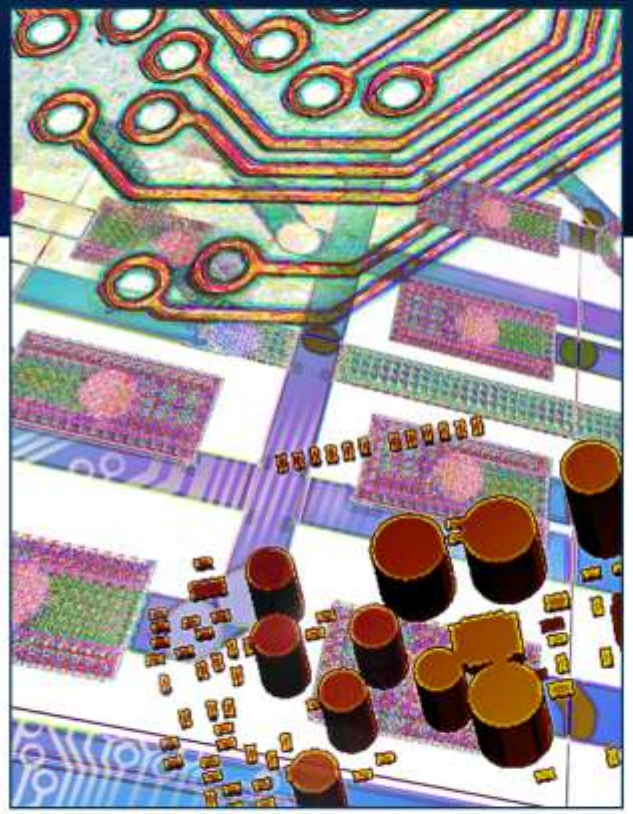


HyperLynx Product Update

Steve Gascoigne

Application Engineer Consultant

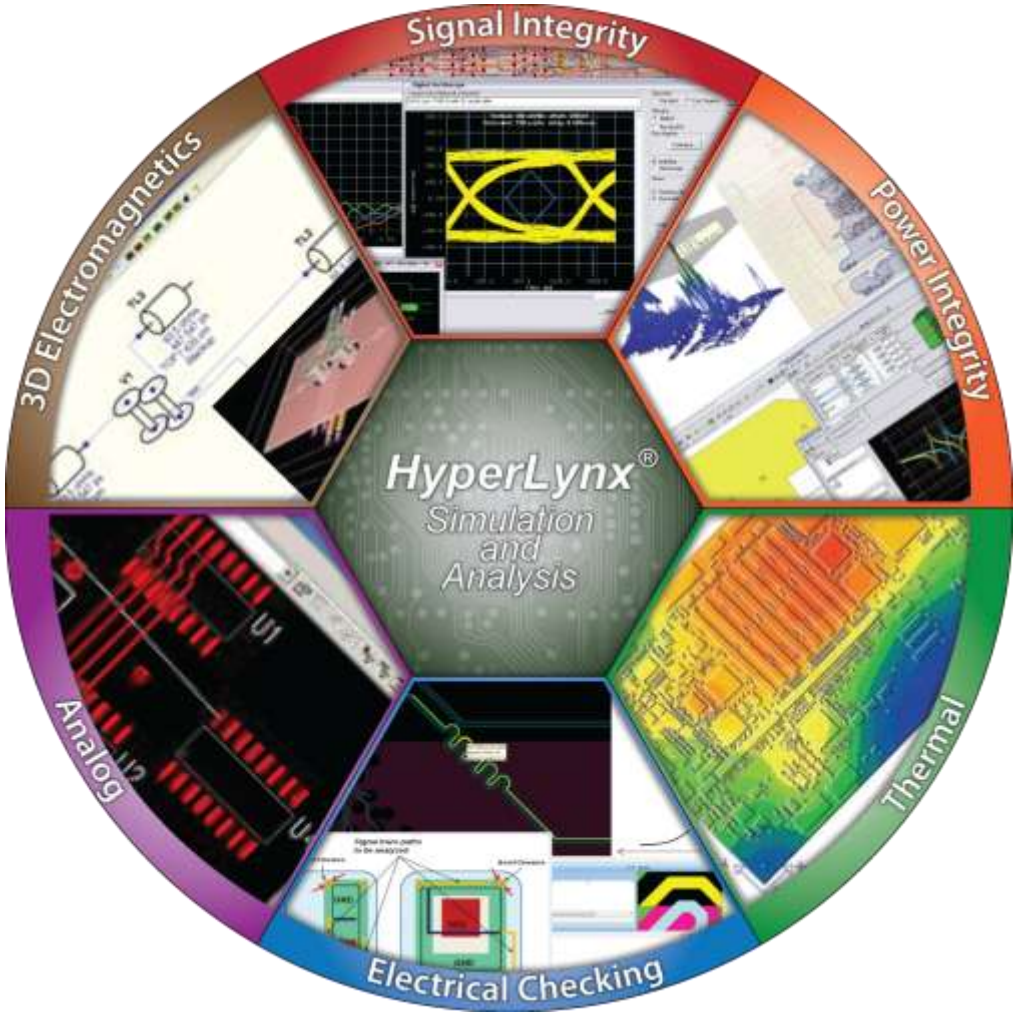
Global Distribution Channel

November 2012

Mentor Graphics®

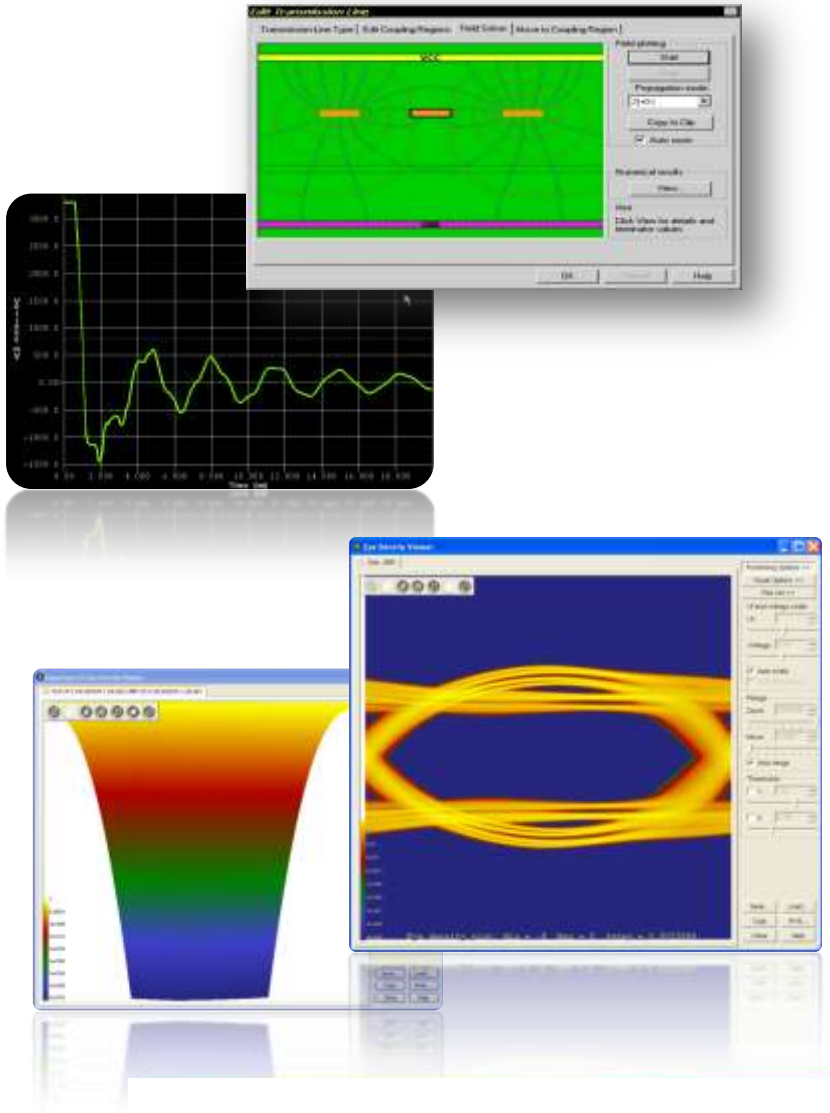
A Complete Analysis Solution

- Address multiple design areas through virtual prototyping
- Integrated technologies to accelerate adoption
- Ease-of-use enables ALL engineers to perform analysis
  - PCB designers thru SI/PI specialists



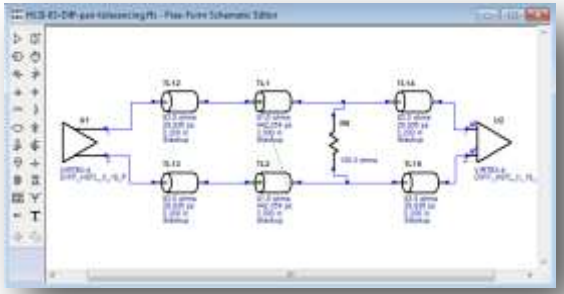
Signal Integrity Concerns

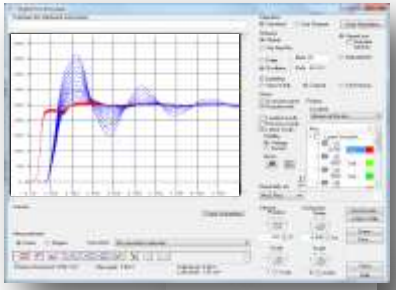
- Traditional signal integrity
  - Crosstalk, overshoot, timing, impedance
- DDRx design
  - Timing, ODT selection
- Multi-gigabit SerDes technologies
  - Loss management, via design, length matching, impedance discontinuities

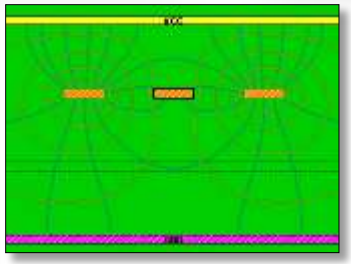


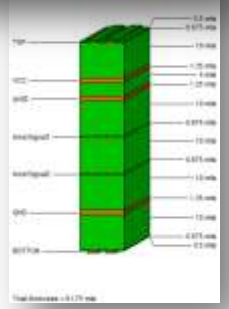
HyperLynx: LineSim SI

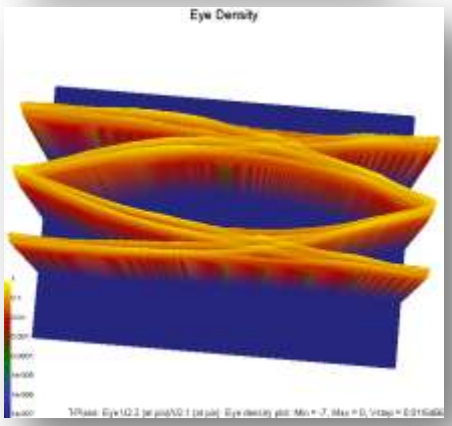
- Industry-renowned ease of use
- Accurate modeling of trace impedance, coupling, and frequency-dependent losses
- Terminator wizard recommends optimal termination strategies
- Identify SI issues, perform crosstalk analysis, parametric sweeps
- Stackup planning
- Integrated timing analysis for DDR, DDR2, and DDR3
- Industry-leading support for high-speed serial interface (SERDES), including fast eye diagram analysis, S-parameter simulation, and BER prediction
- Advanced via modeling
- Provides an early look at likely EMC failures
- Integration with the constraint editing system

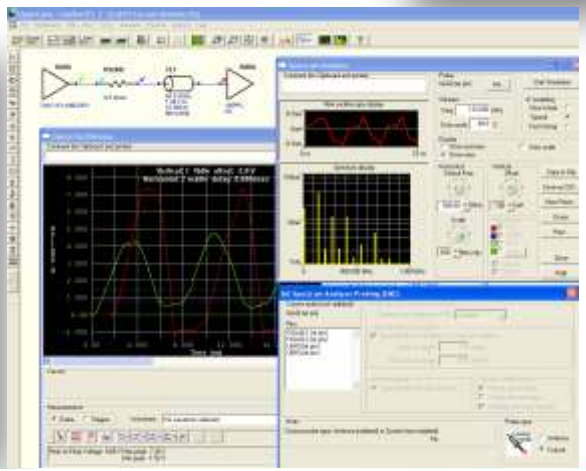






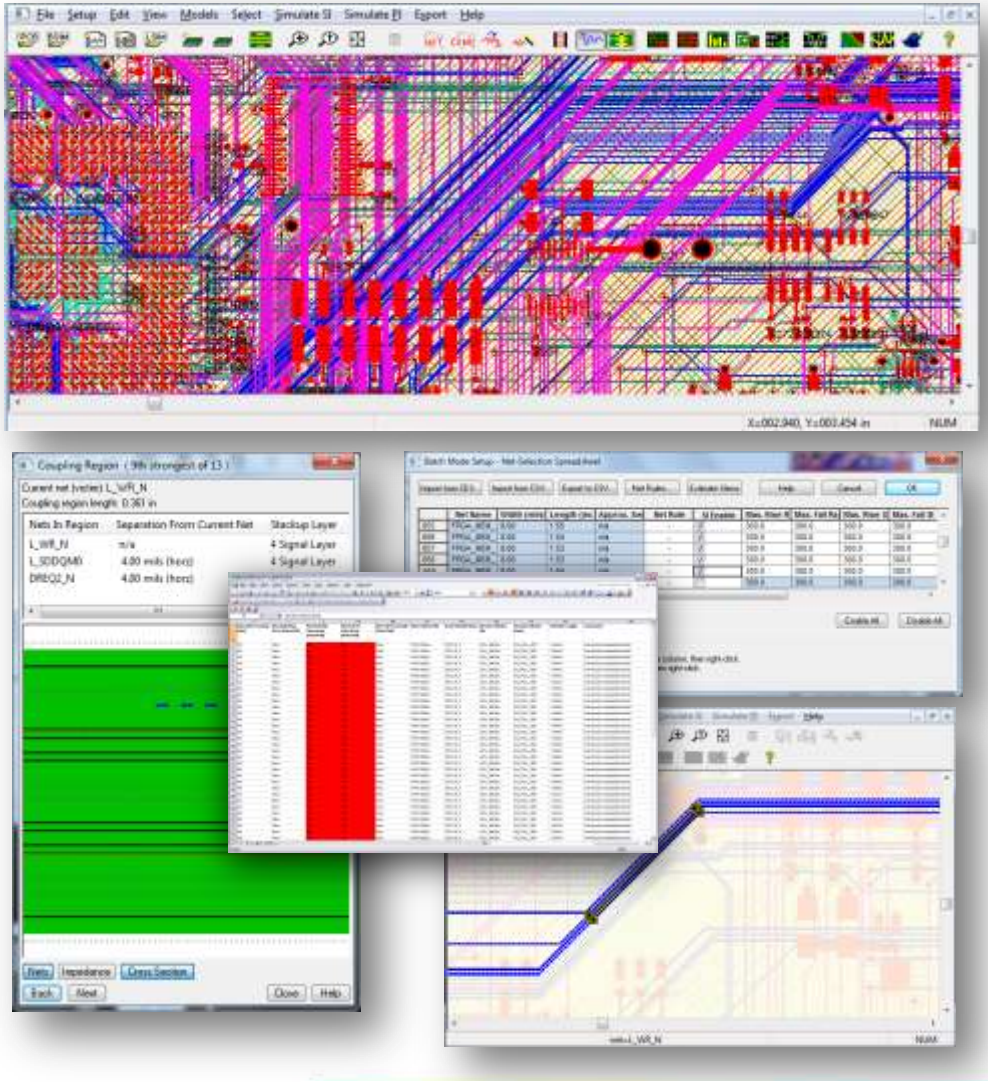






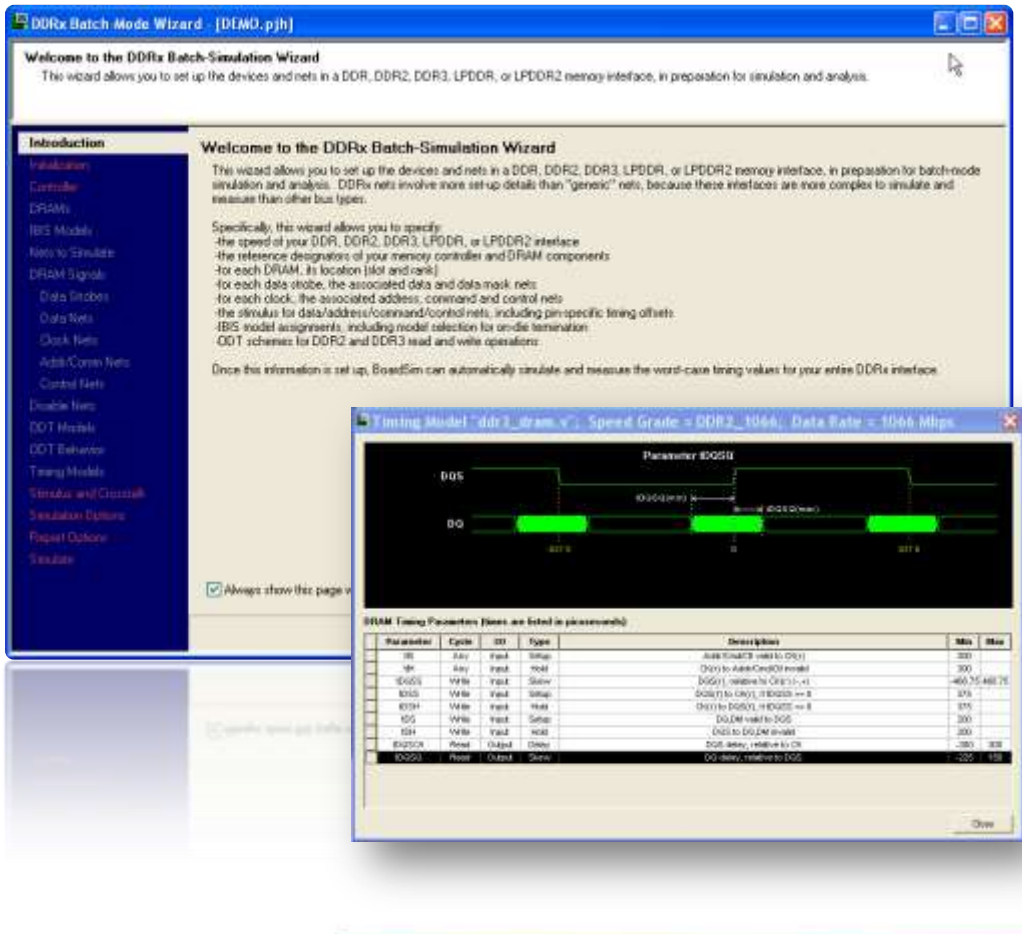
HyperLynx: BoardSim SI

- Simulate post-routed data from your host PCB system
- Run interactive simulations on individuals nets
- Run a comprehensive batch simulation on many nets at once
- Parametric sweeps
- Verify DDR/2/3 bus structures (single and multi-board setups)
- Crosstalk analysis
- Advanced Timing Analysis
- Interactive EMC Analysis
- Run SERDES Fast-eye analysis
- Run IBIS-AMI channel analysis



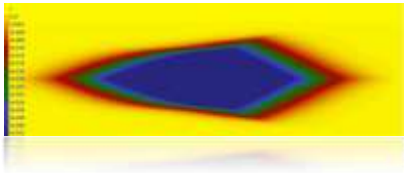
HyperLynx DDRx Simulation

- Validate LPDDR and DDRx timing and SI designs
  - Analyze timing for both address and data buses
  - Measurements for clock to strobe skew
  - Measure timing and SI on all signal edges
  - Advanced crosstalk simulation
- Analysis is simplified through an interview process

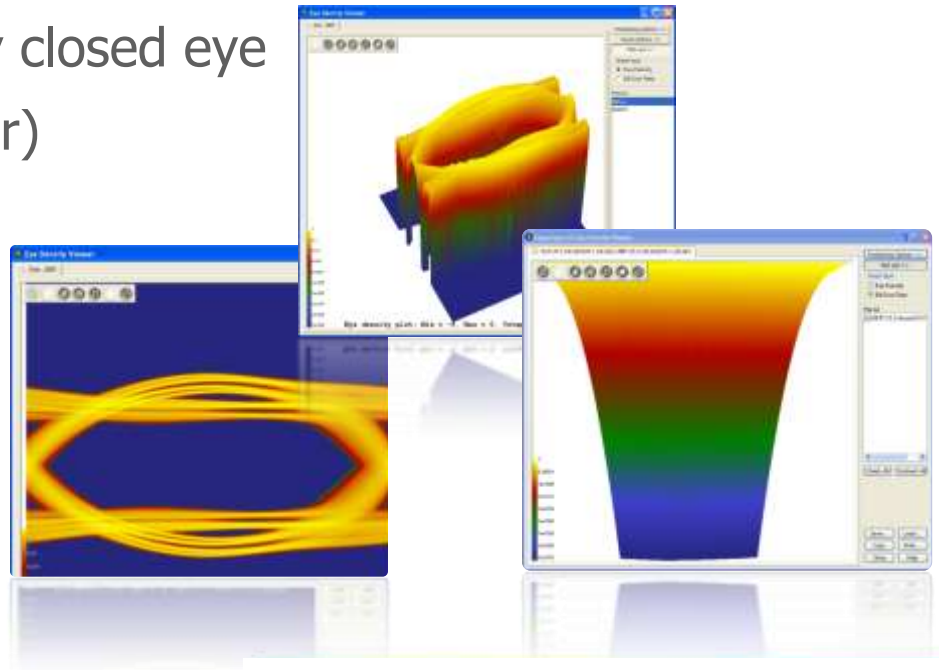


Multi-Gigabit Channel Analysis

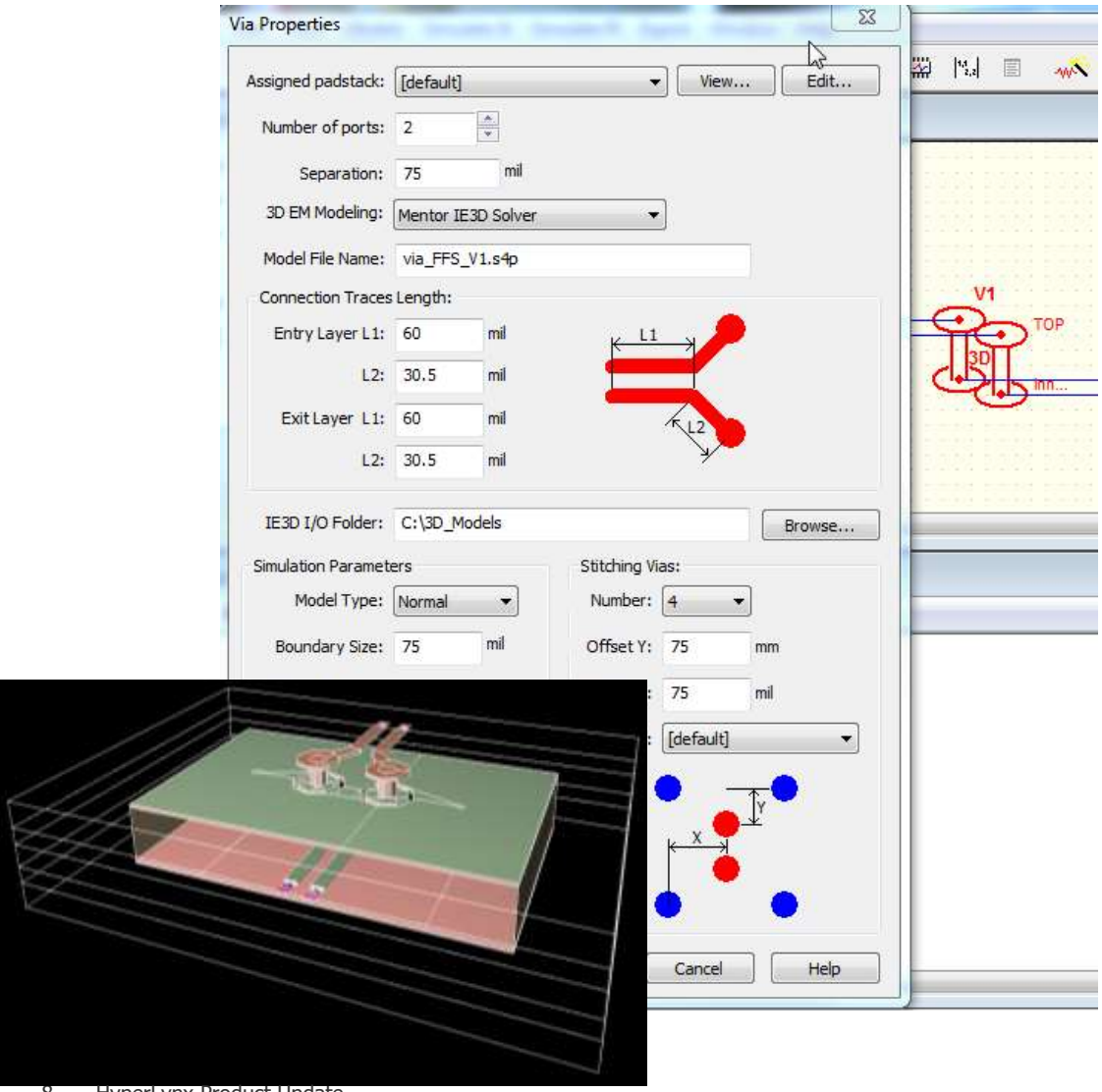
- Fast time domain and statistical analysis
  - Simulate millions to billions of bits for accurate BER prediction



- Generate the channels worst case bit sequence
  - PRBS or 8B/10B protocol dependant
  - Always produces a maximally closed eye
  - Bounds Dj (deterministic jitter)
- Validate BER
  - Eye density plots
  - BER plots
- Support for IBIS-AMI, SPICE, S-Parameters



Full-Wave 3D Via Modeling



- Some designs require more accurate via models
  - Can contribute significant loss at higher frequencies
- Need the ability to accurately tune the via design
  - Separation, stitching, entry angle, etc.
- 3D simulation provides highly accurate models up to 100+ Gbps frequencies

3D Full-Wave EM Modeling

HyperLynx 3D EM

- Based on IE3D technology
  - Fastest, highest-capacity, full 3D EM simulation in the market
- NEW product for Mentor Graphics
  - Zeland Software, Inc. acquired February 2010
- Creates high-frequency parasitic models needed for circuit simulation
  - Frequency-dependent parasitic extraction of metallic structures – "s-parameter models"
- Highly respected for EM design & verification
  - Over 1600 customers
  - Long history (since 1992) of production proven use

$$\oint_C \vec{E} \bullet d\vec{S} = \frac{q}{\varepsilon_0 \varepsilon_r} = \Phi_E$$

$$\oint_C \vec{B} \bullet d\vec{S} = 0 \quad \oint_C \vec{B} \bullet d\vec{S} = \Phi_B$$

$$\oint \vec{E} \bullet d\vec{l} = -\mu_0 \mu_r \frac{d\Phi_B}{dt}$$

$$\oint \vec{B} \bullet d\vec{l} = \mu_0 \mu_r \left(\varepsilon_0 \varepsilon_r \frac{d\Phi_E}{dt} + i \right)$$

Employs a Unique 3D Integral Equation Method to Solve Maxwell's Equation Governing Electrical Behavior of Metallic Structures

Application of HyperLynx 3D EM

EM Simulation is Used in All High-Frequency Design Applications

- Wireless
  - Cell phone, routers, Bluetooth, GPS, LTE, wimax (802.16)
  - Antenna and antenna arrays
  - RFID/zigbee tag design
- Hi speed digital
  - 10G/40G+ internet, Fibrechannel, XAUI, PCIE, Infiniband
  - On-chip SerDes, package
  - DDR2/DDR3 memory I/F channel
- Military/aerospace
  - Secure communications/network
  - Large phase array/imaging antenna
  - Compact multi-band antenna
  - Materials research

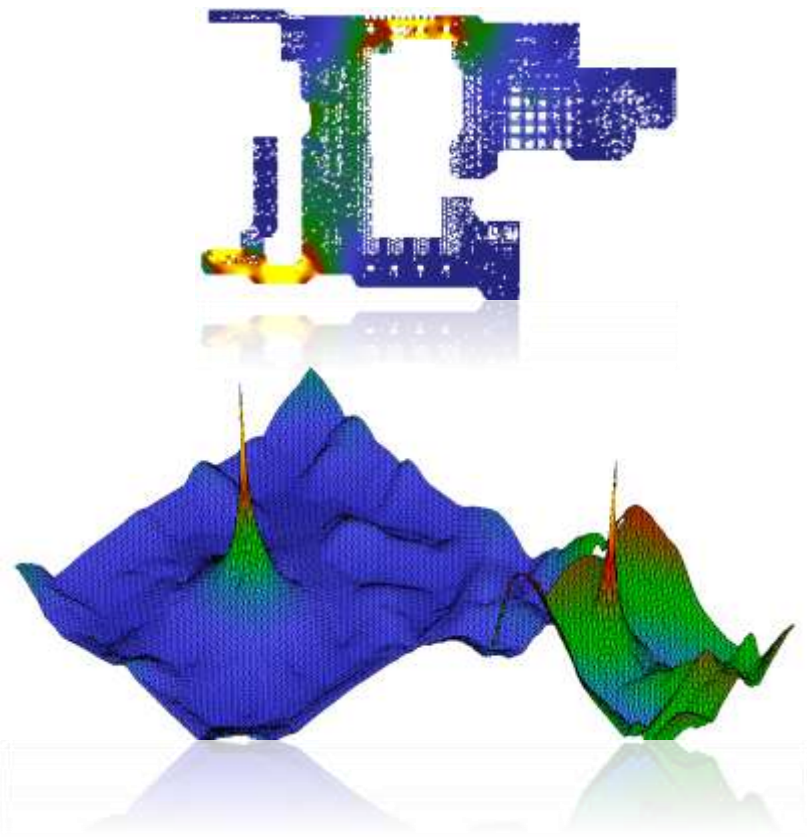
HyperLynx 3D EM Value

Fastest commercial 3D EM simulator
Has the largest design capacity
Accuracy matches measurement
Packaged for widespread deployment

- Fastest EM design closure
  - More simulations/hour accelerates design convergence
  - Higher capacities alleviate need to manually partition design
- Lower EM design costs
  - Unique, scalable distributed EM simulation
  - Replace less-capable, more-expensive competitive alternatives
  - Reliable, predictable results reduces risks of costly design iterations
- Improve design quality - minimize EM design re-spins
  - Higher simulation coverage helps ensure nothing was missed
  - Higher capacity – detect hard-to-find EM design flaws prior to prototype
  - Reliable, predictable results increases designer confidence

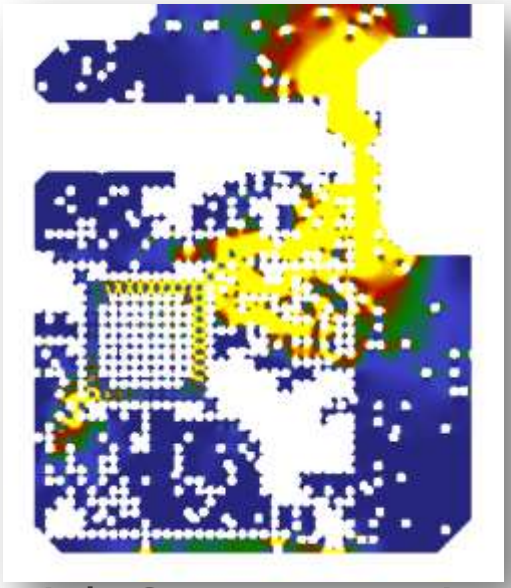
Power Integrity Analysis

- DC drop analysis
  - Identify excessive voltage drop and high current densities
  - Determine if there is enough copper & stitching vias
  - Batch analysis of all power nets
- AC power plane analysis
  - Optimize capacitor selection and mounting
  - Verify power supply impedance at IC power pins
  - Analyze voltage ripple on power nets

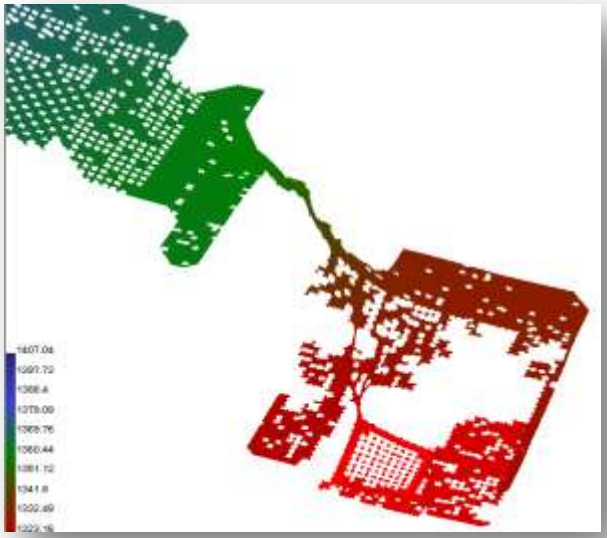


IR Drop Design Issues

- Common problems:
  - Not enough voltage getting to ICs from power supplies
    - Leads to IC malfunction
  - High current densities in voltage island neck-downs and vias
    - Leads to dielectric or via breakdown and board failure



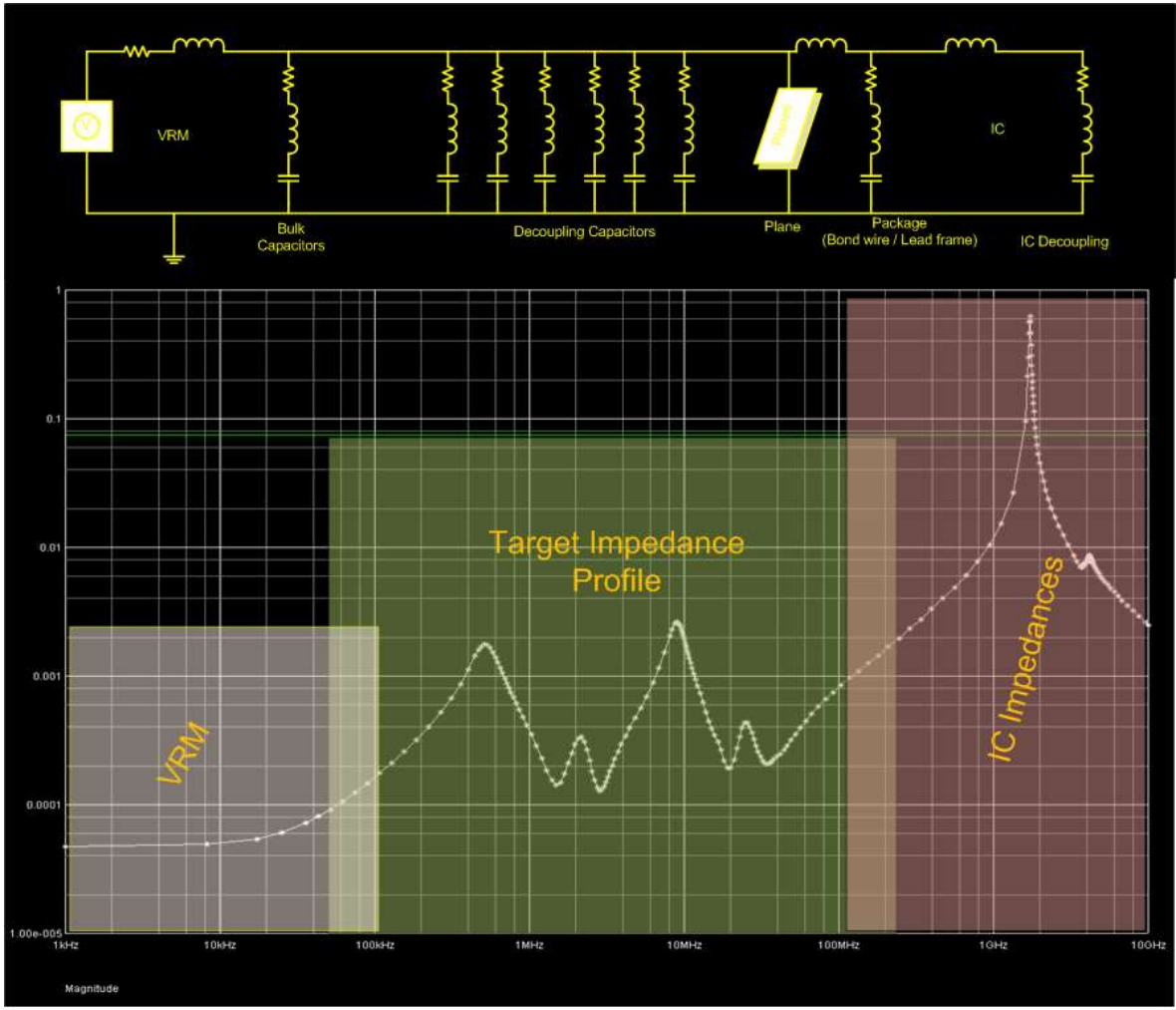
High Current Density



Excessive Voltage Drop

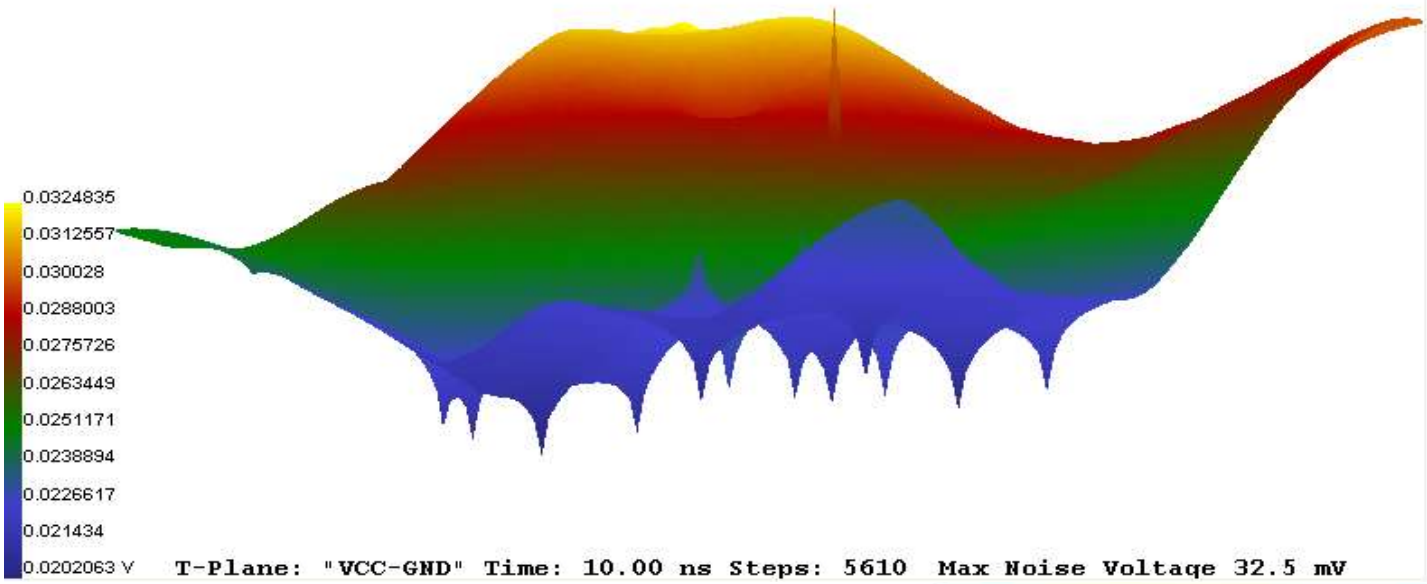
Decoupling Design

- Develop decoupling methodologies to
  - Properly design stackup for power
  - Design capacitor mounting structures
  - Make intelligent capacitor selections
- Goal = Achieve IC Target Impedances for power
  - Set by voltage ripple requirements



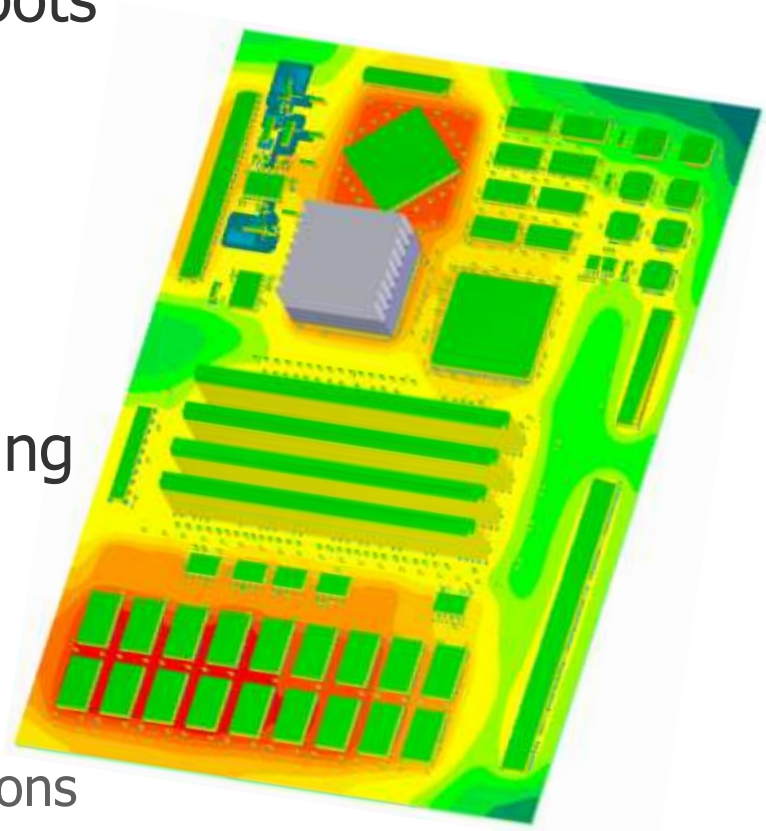
Plane Noise Analysis

- HyperLynx Plane Noise can help identify voltage ripple exceeding IC power pin specifications
- Plane noise is a result of target impedance and switching currents
  - (V=I*R)
  - Amount of voltage noise is dependant on edge rate (frequency) of current and impedance at that frequency



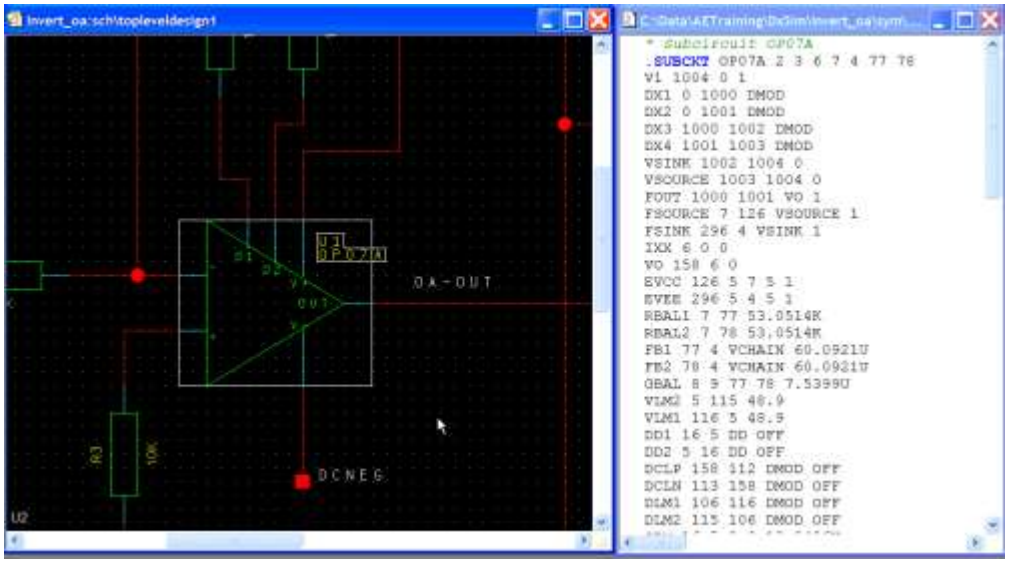
Thermal Analysis

- Allows engineers and PCB designers to identify component and PCB hot spots
- What-if analysis on
  - Component placement
  - Stackup design
  - Mechanical cooling techniques
- Quick and accurate analysis including
  - All PCB copper
  - Packages, Pins, vias, screws, etc
  - Environment including enclosure
  - Package to Board, Pin to Board junctions
  - Heat sinks and Airflow



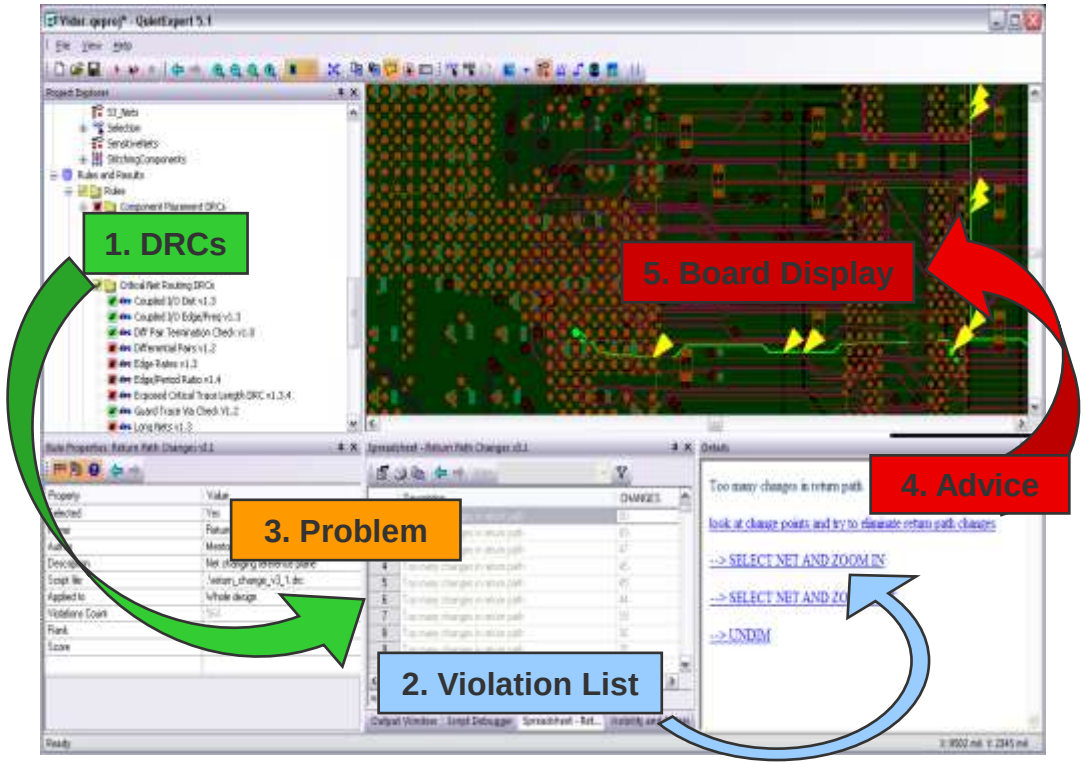
Analog Simulation

- Scalable simulation solution built on DxDesigner
- Analog and full mixed signal simulation capability
  - — Support for analog and digital primitives
  - — Standard language support
    - – VHDL, VHDL-AMS, Spice, & Verilog-A
  - — Power ADMS and Eldo simulation kernels
- Full featured waveform viewing with EZWave
  - — Including complex waveform calculations



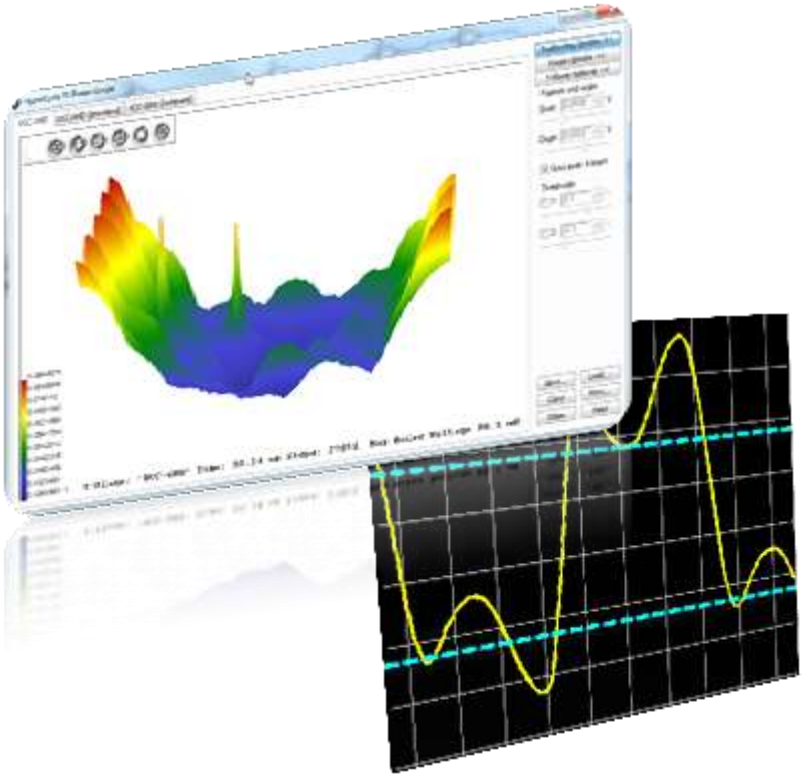
EMI / PCB Verification

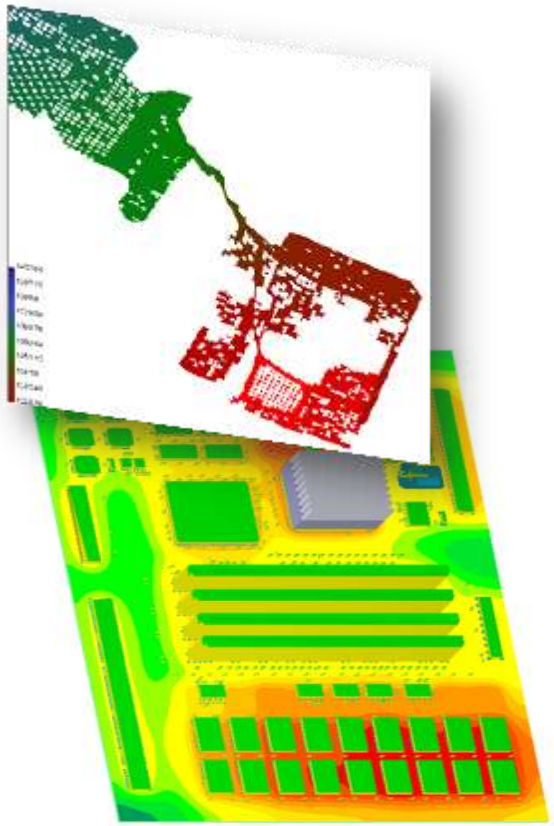
- PCB Design Validation
  - Rules-based verification of the PCB
  - Finds problems before building prototypes
  - Create custom design rules to identify **your** common problems
- Automates the design review process
  - Enables consistency
  - Minimizes human error
  - Reduces design review time investment



Crossing Domains

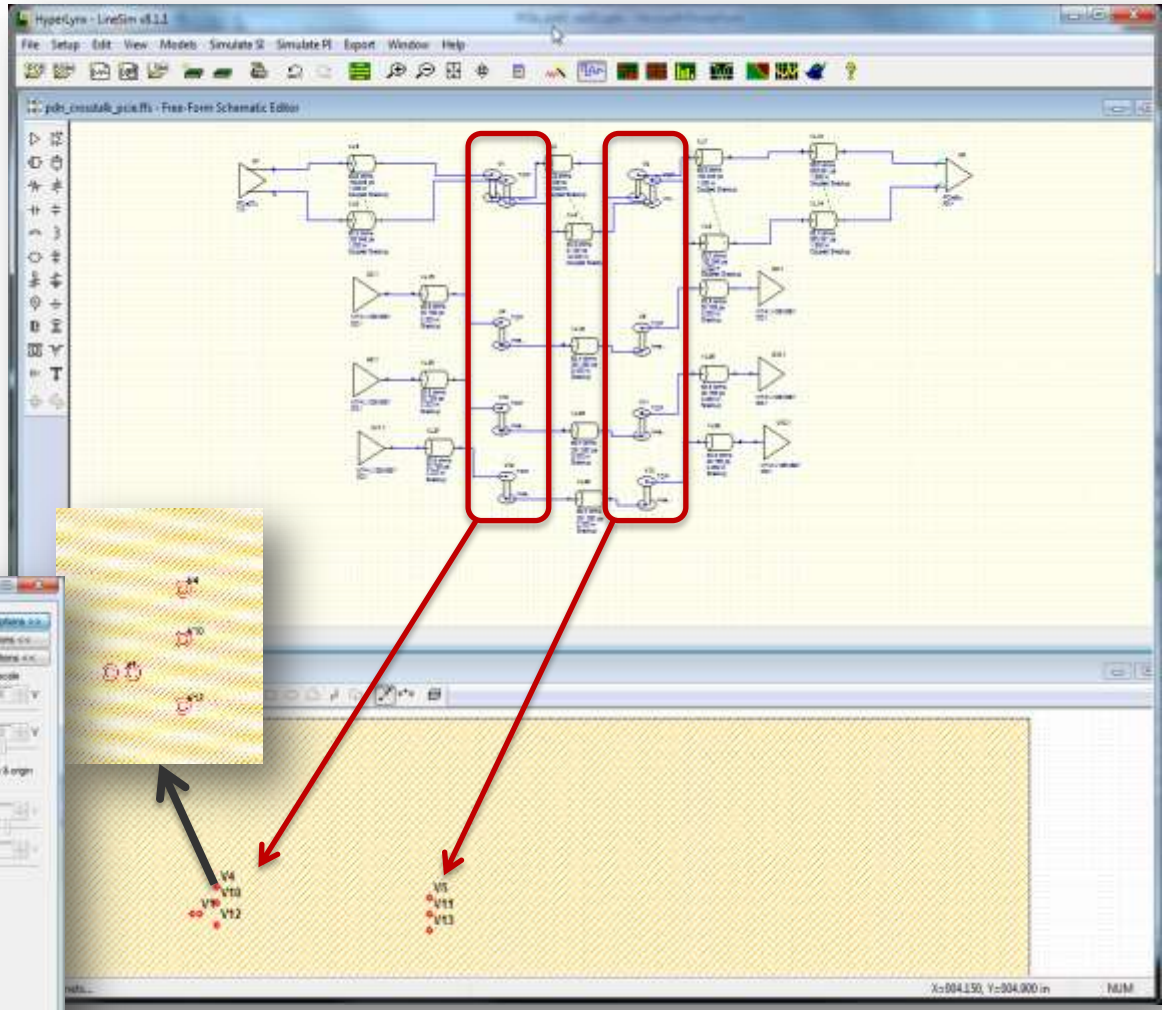
- Sometimes independent analysis addresses only part of the issue
- Integrated Analysis flow allows for simulation across domains

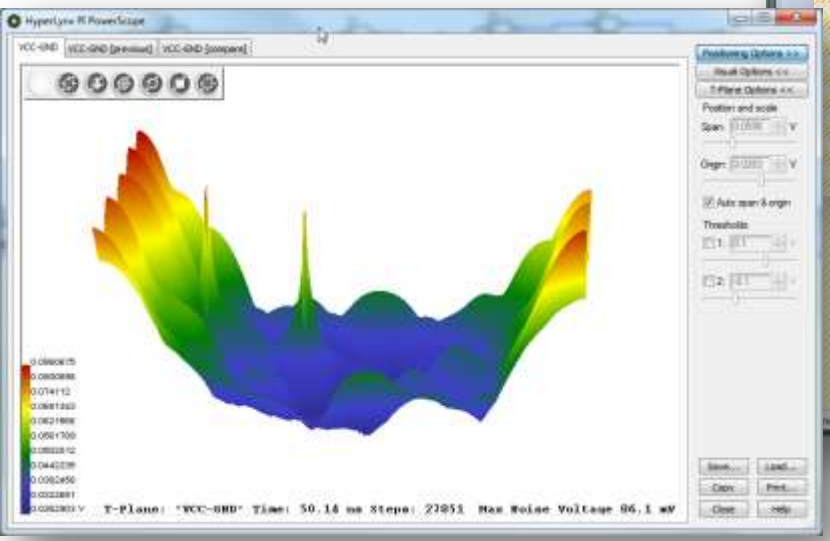




Simulating Via-to-Via Crosstalk

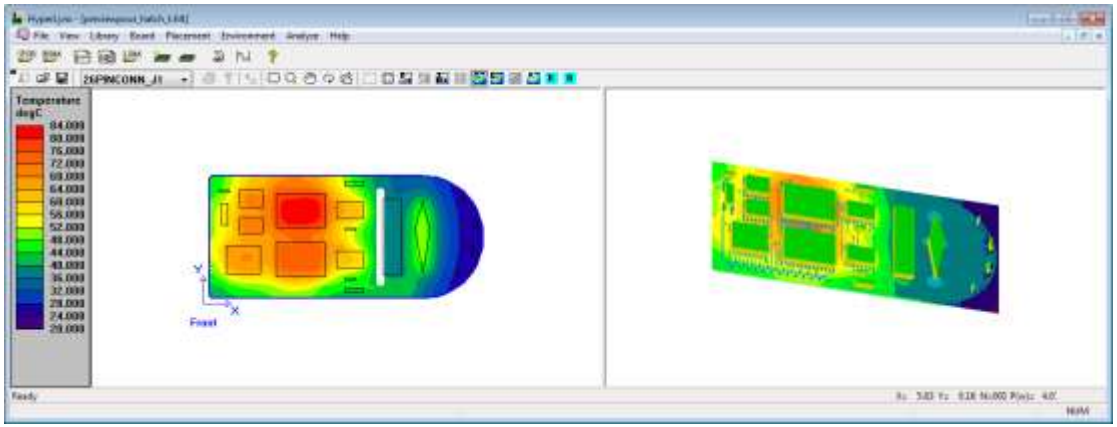
- Mixed signal and power integrity simulation
  - Via crosstalk through power planes





PI/Thermal Co-Simulation

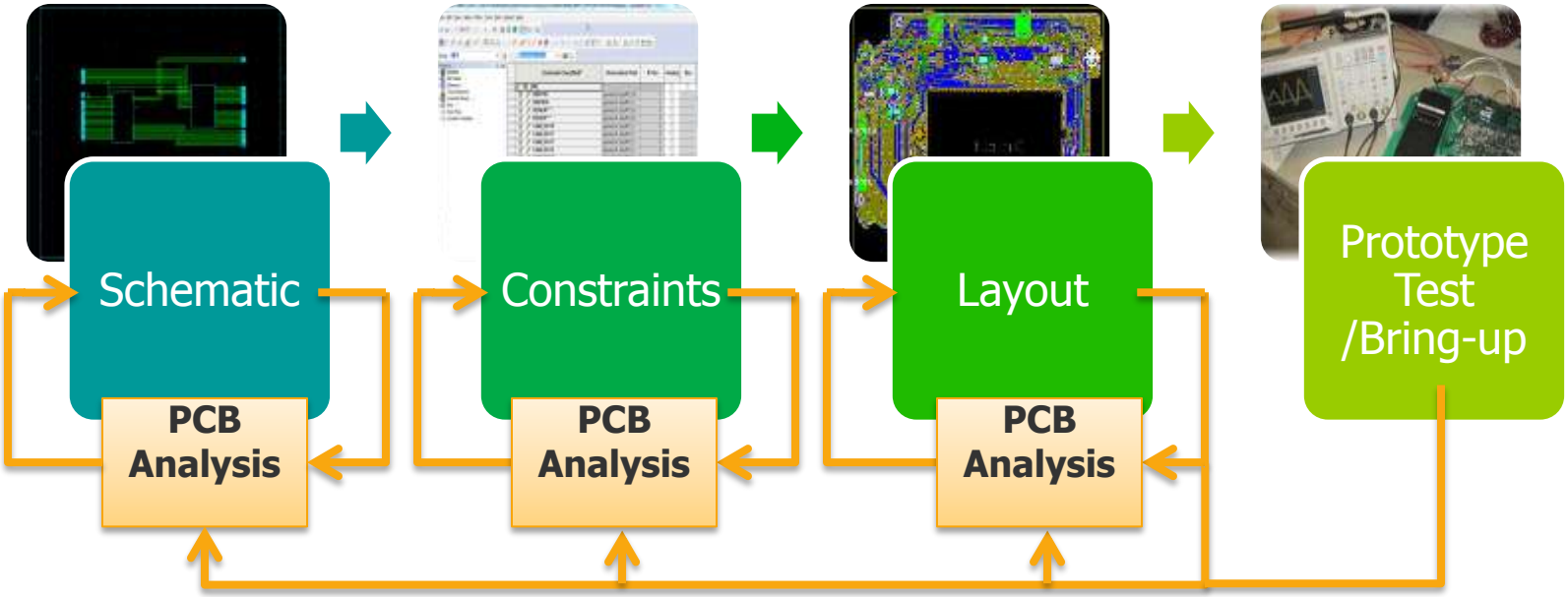
- HyperLynx Thermal within the existing HyperLynx SI and PI environment
- Co-Simulation capabilities between PI and Thermal
  - Power Integrity engine (DC drop) simulates power nets provides power density "map" to thermal solver
  - Thermal solver runs thermal analysis with component power dissipation and results from PI simulation
  - System runs several iterations of above process with PI simulator using updated resistances(based on temp) until convergence



Analysis is Core to the Design Process

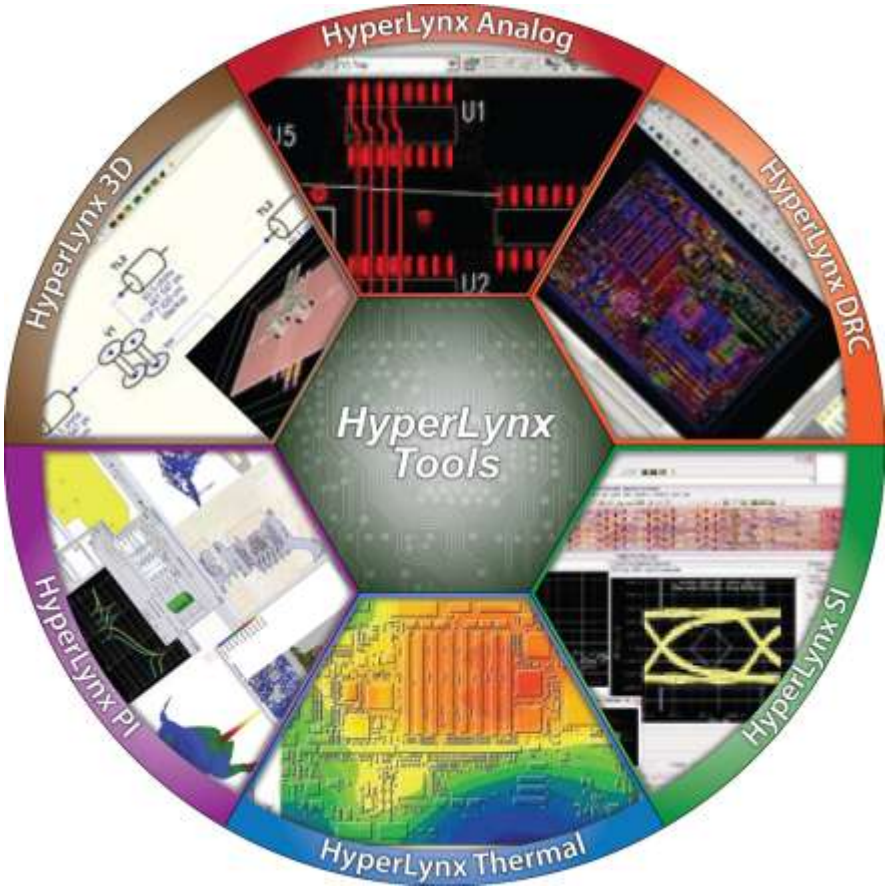
- PCB design is more than schematic and layout
  - We know designs are becoming more complex
- To meet reliability and time-to-market
  - Project engineers must do PCB Analysis

"HyperLynx is now mandated as part of our PCB design process."
- SEAKR Engineering



HyperLynx Analysis Environment

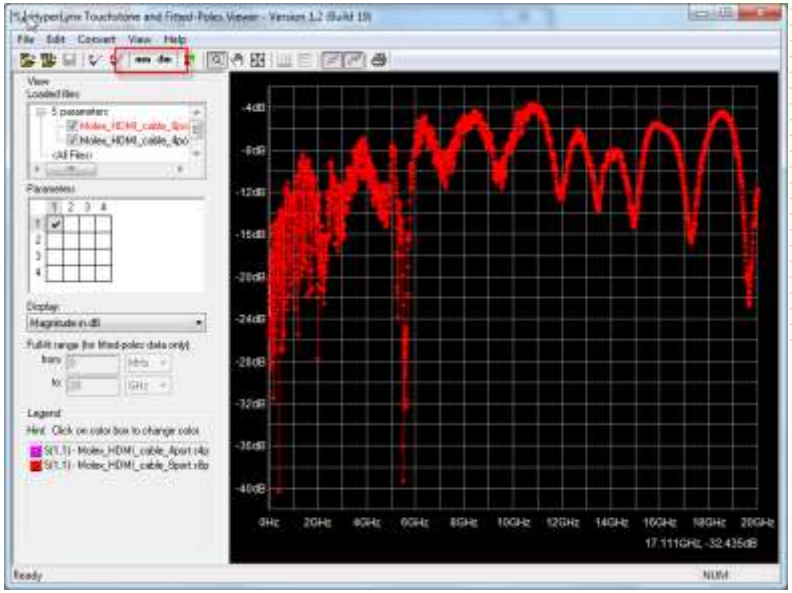
- Comprehensive suite of analysis technologies
  - Reduce design cycle time
    - Develop constraints for "first time right" design
  - Improve design reliability
    - Validate design intent before prototyping
  - Verification in multiple domains
    - Accurate & fast time-to-results
  - HyperLynx enables ALL engineers to drive analysis

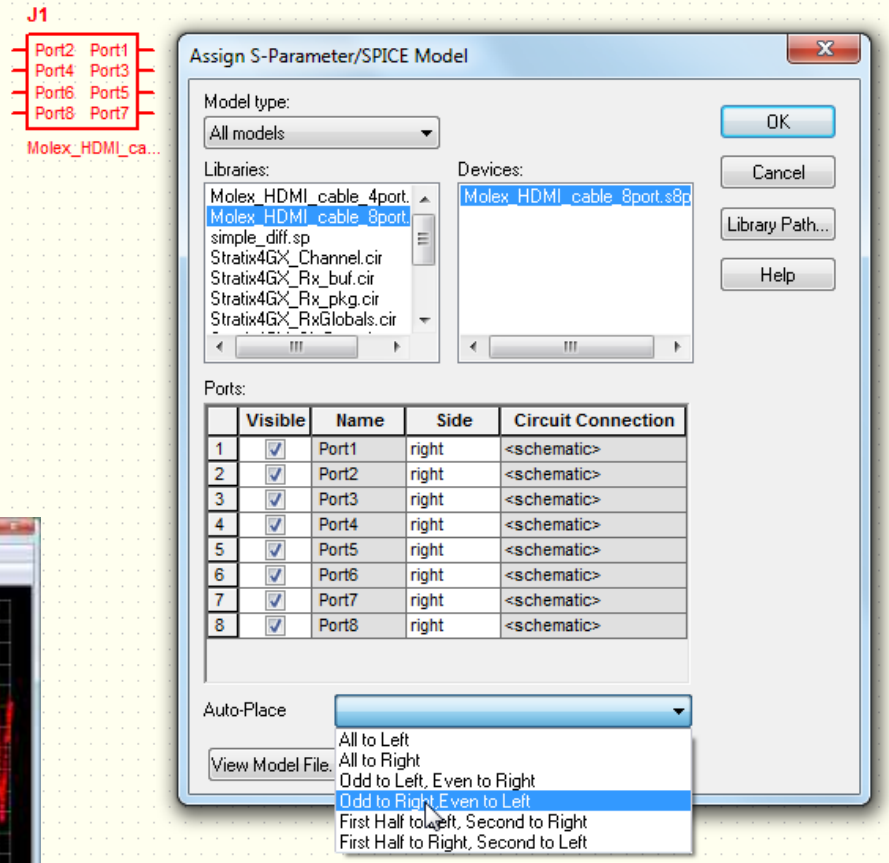


SI Enhancements

8.2

- Usability improvements
  - Auto placement of s-parameter ports in LineSim
  - Easy generation of mixed-mode and differential-mode S-parameters

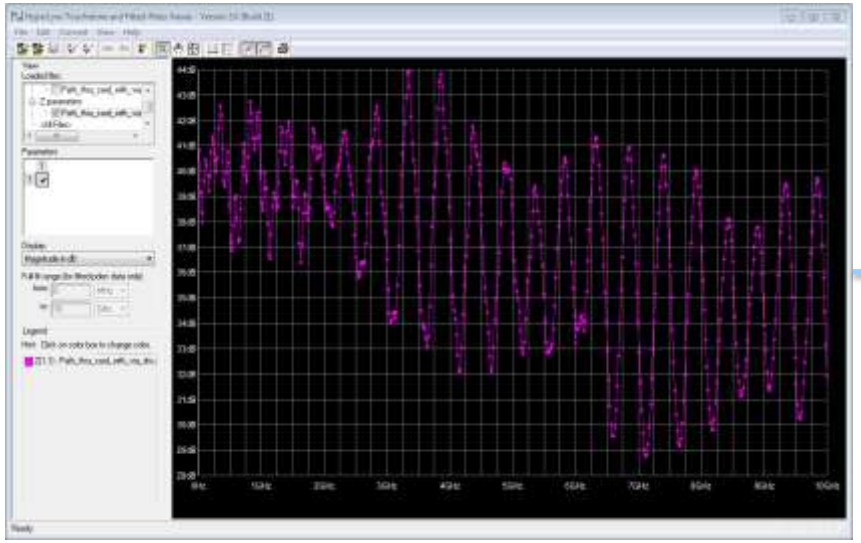


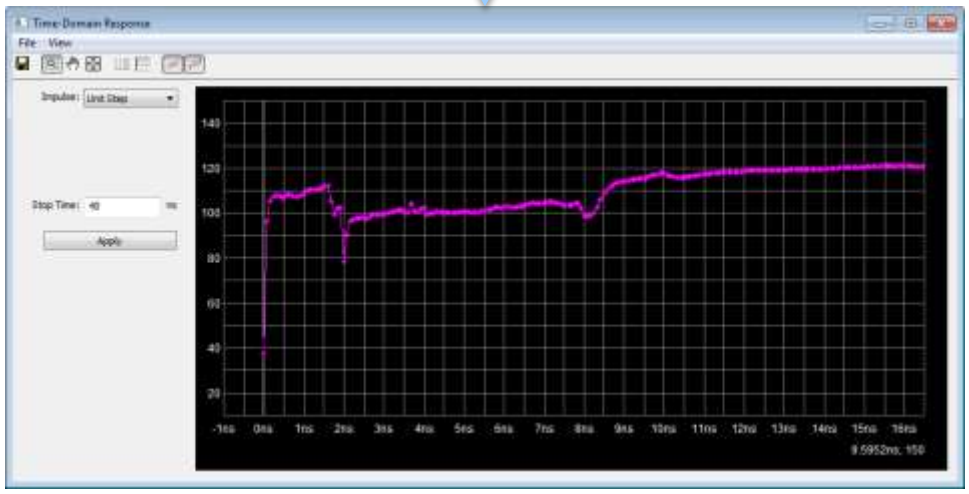


SI Enhancements

8.2

- Time domain view of S/Y/Z data from Touchstone Viewer

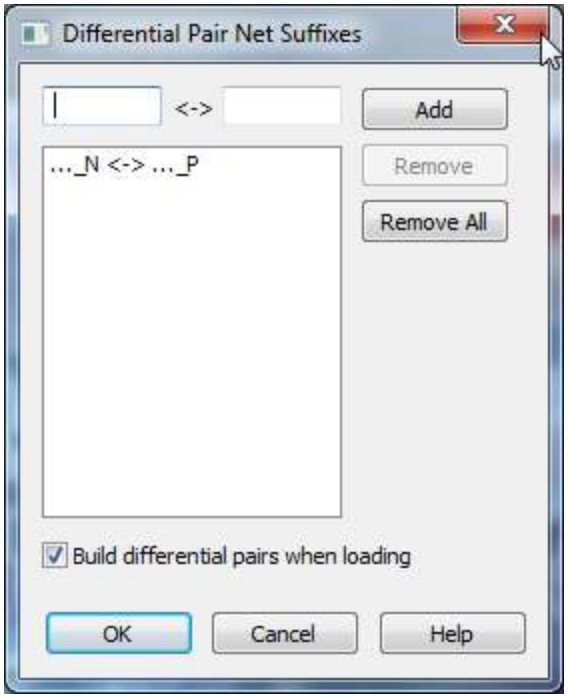


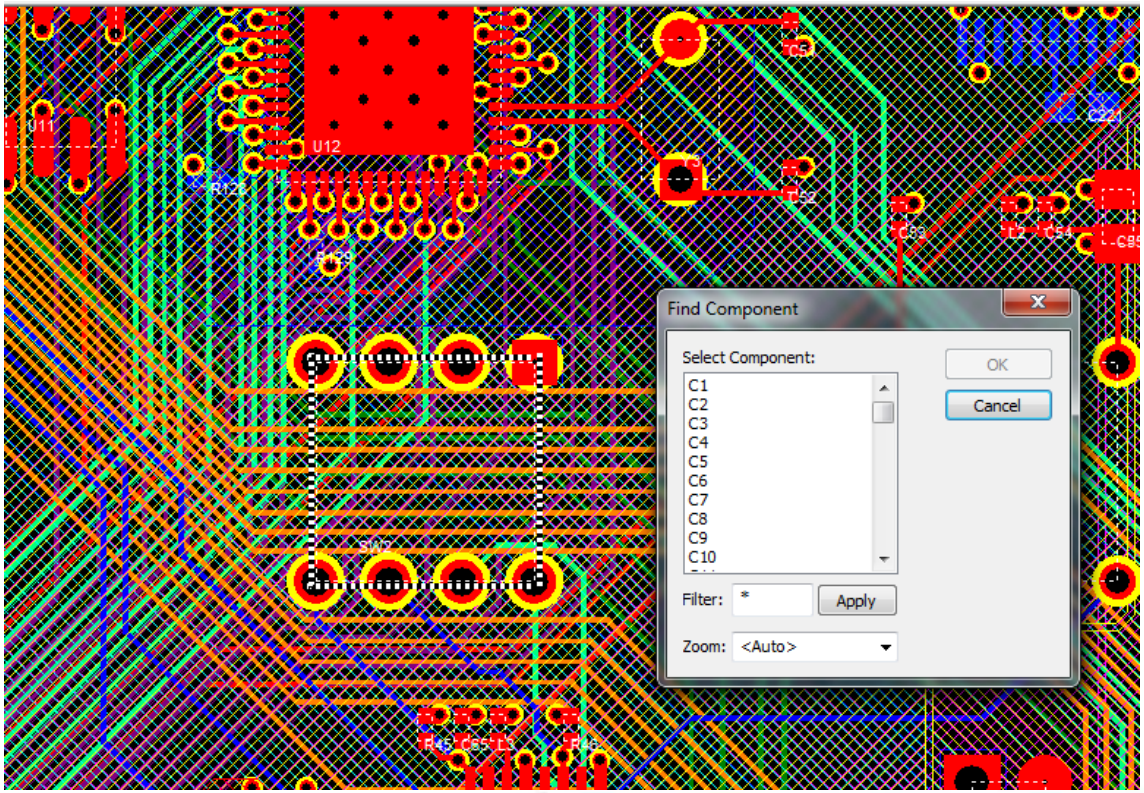


SI Enhancements

8.2

- Usability improvements - BoardSim
  - Quickly find components
  - Automatic association of diff-pairs by net name

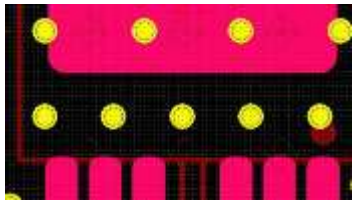


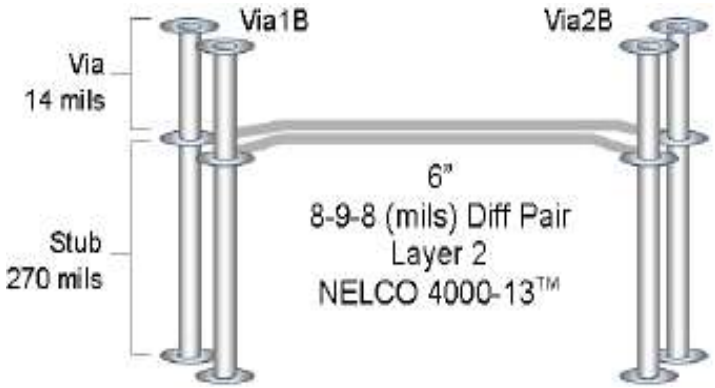


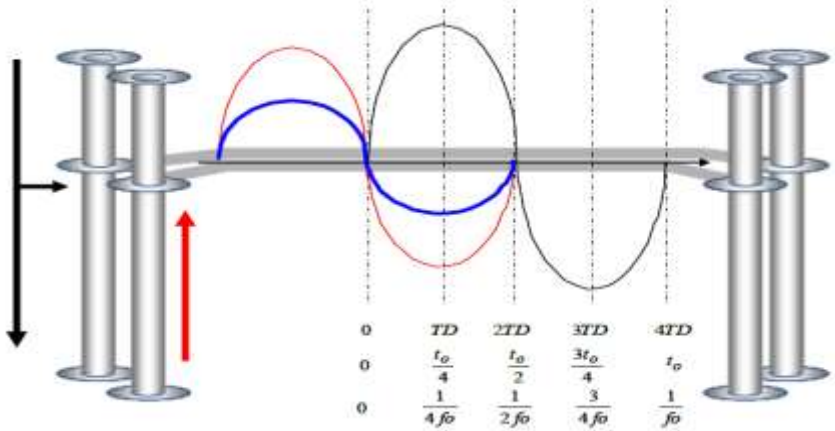
SI Enhancements

8.2

- Multi-gigabit channel design Improvements
  - Export of via-in-pad from BoardSim to LineSim
  - Support for custom pad shapes
    - Both viewing and electrically
  - Improve via models (add stub L, etc.)
    - Current stub modeling does not include L (only C)





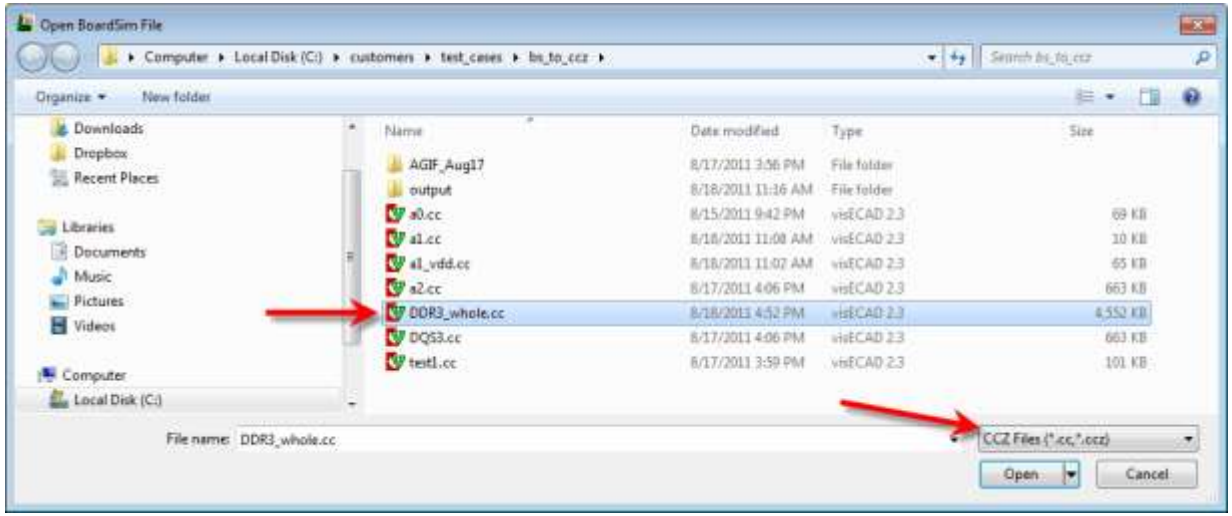


SI Enhancements

8.2

Open/Import .ccz data within BoardSim

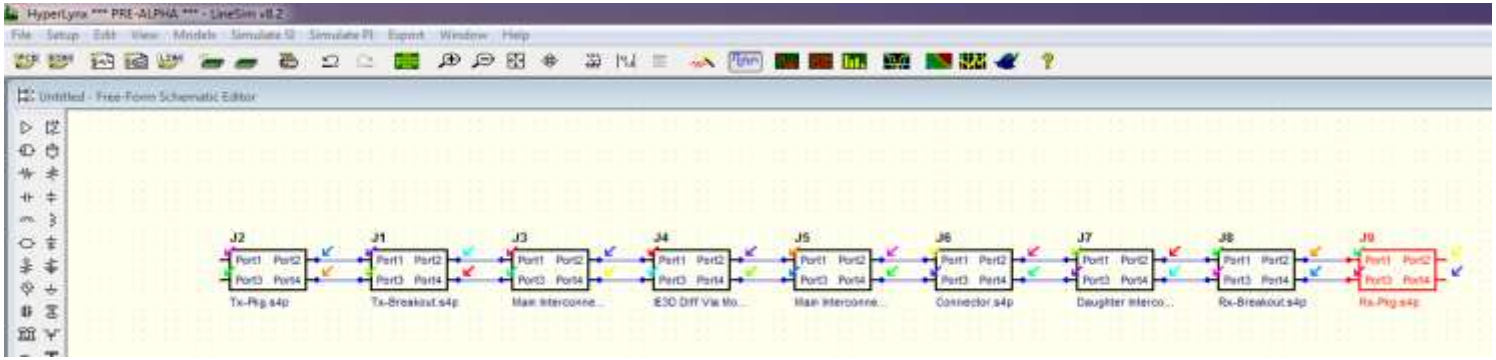
- Adds support for currently unsupported custom pads within the .hyp import to BoardSim flow
- Allows us to leverage CAMCAD translators increasing number of supported design/layout packages



SI Enhancements

8.2

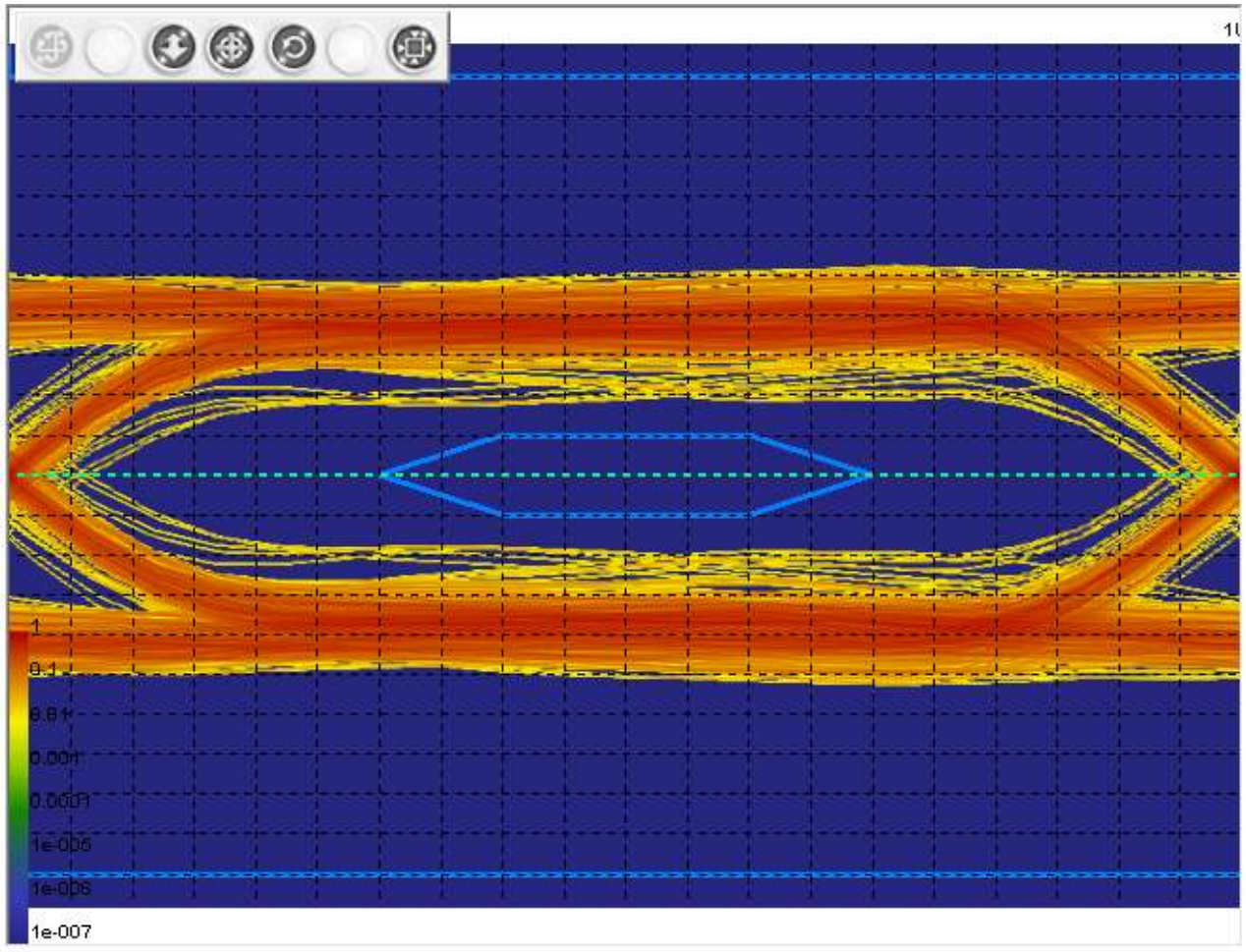
- Cascading S-parameters
  - Chained s-parameter models can cause inaccuracy
    - Different frequency sampling points in models
    - Different frequency range
- Automatic conversion to transfer function
  - Produces high-accuracy composite model



SI Enhancements

8.2

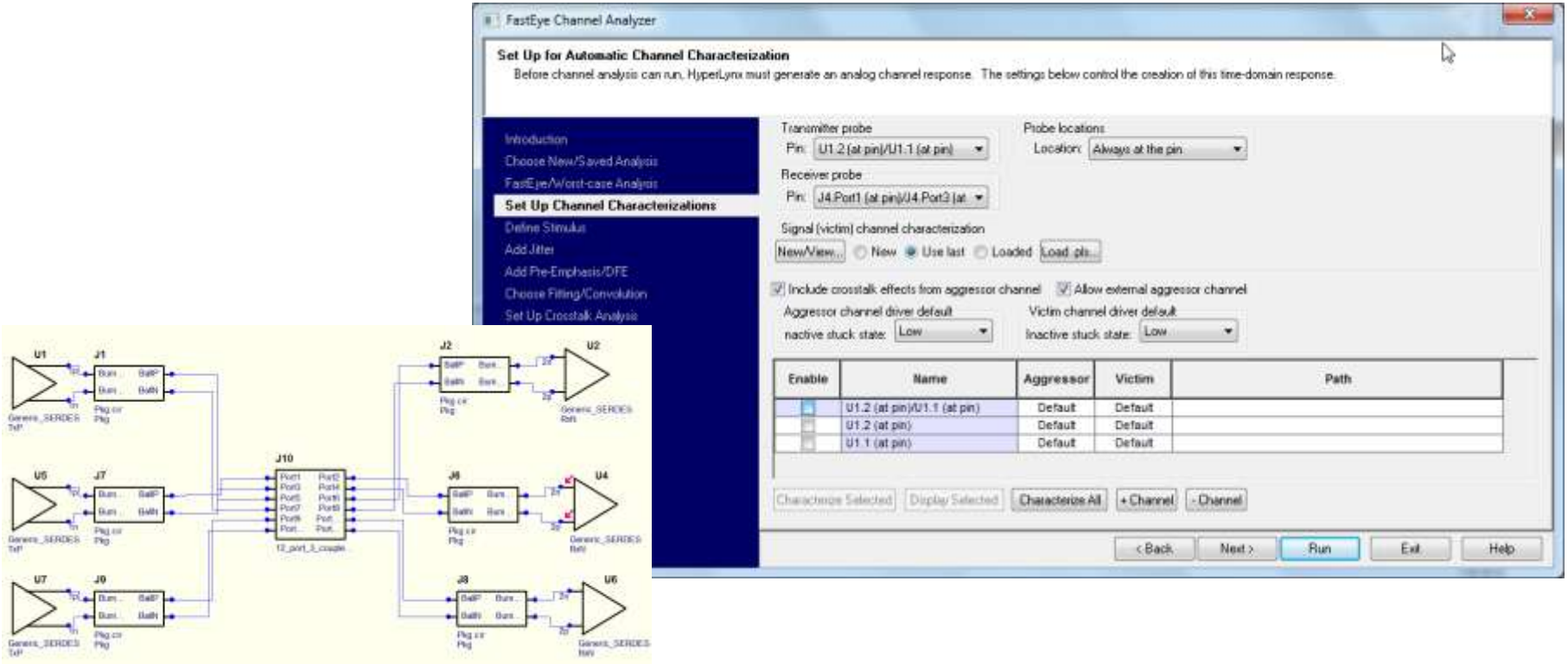
- Improved eye density viewing
  - Eye mask
  - Voltage/time grid



SI Enhancements

8.2

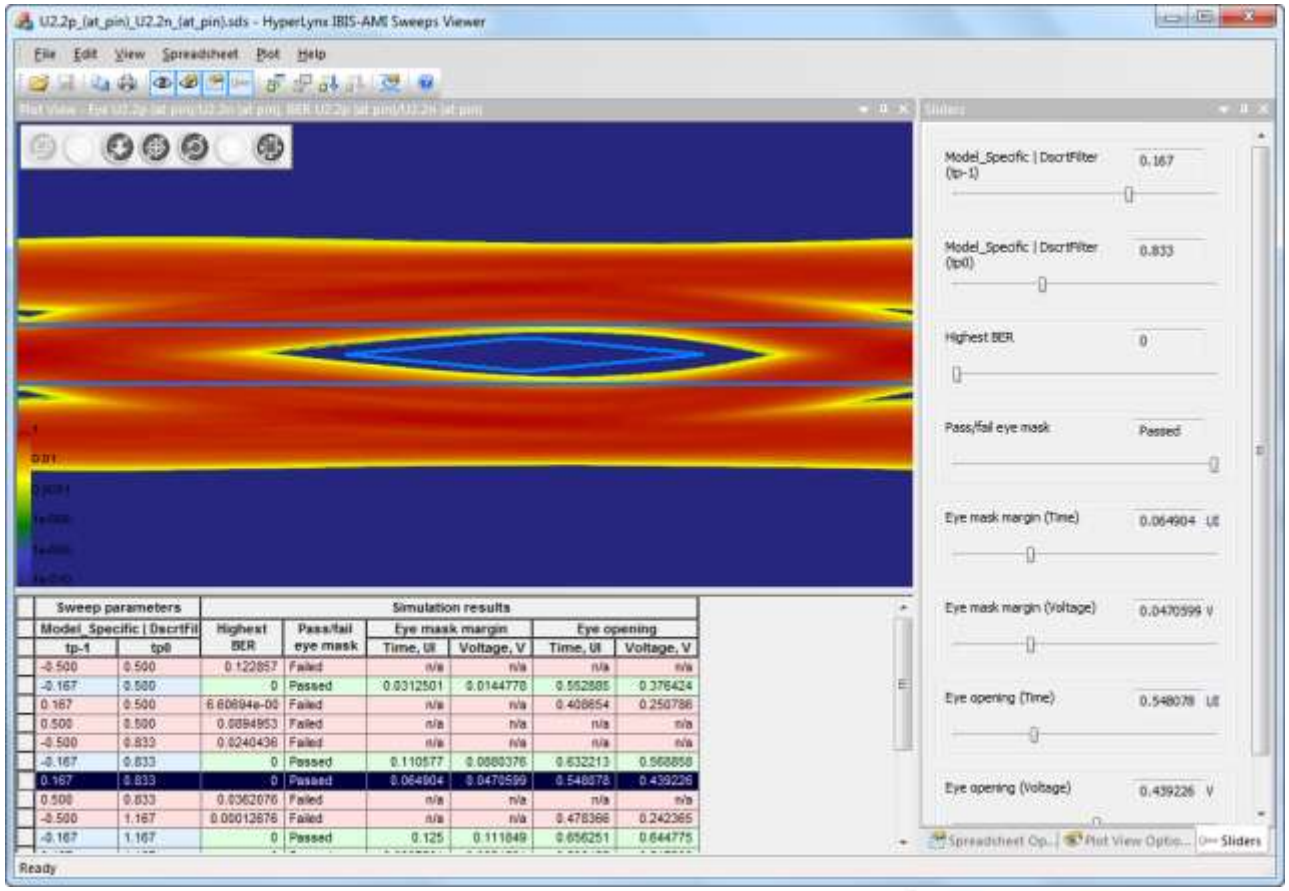
- FastEye and IBIS AMI crosstalk
  - Higher accuracy BER predictions
  - Include asynchronous and synchronous crosstalk effects



SI Enhancements

8.2

- AMI-model parameter sweeping
  - Sweeping allows user to "optimize" channel and I/O for low BER

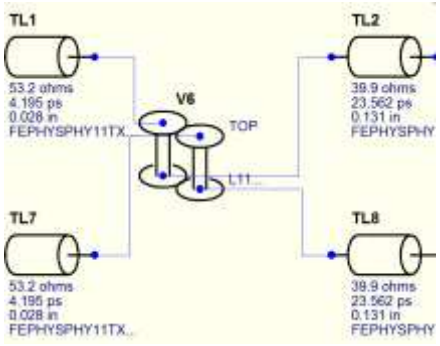


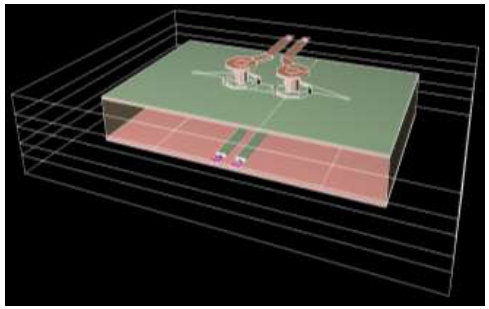
SI Enhancements

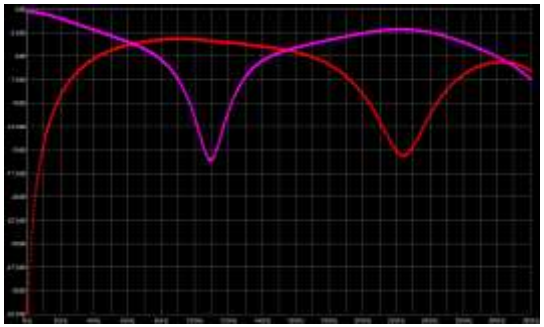
8.2

Integration of LineSim to HyperLynx 3D EM / IE3D

- IE3D technology will help robust high-speed simulations at 10 Gbps and above
  - But in its "native" form, it's much too complex for most customers to understand/use
- HyperLynx will "front-end" the process of 3-D model creation

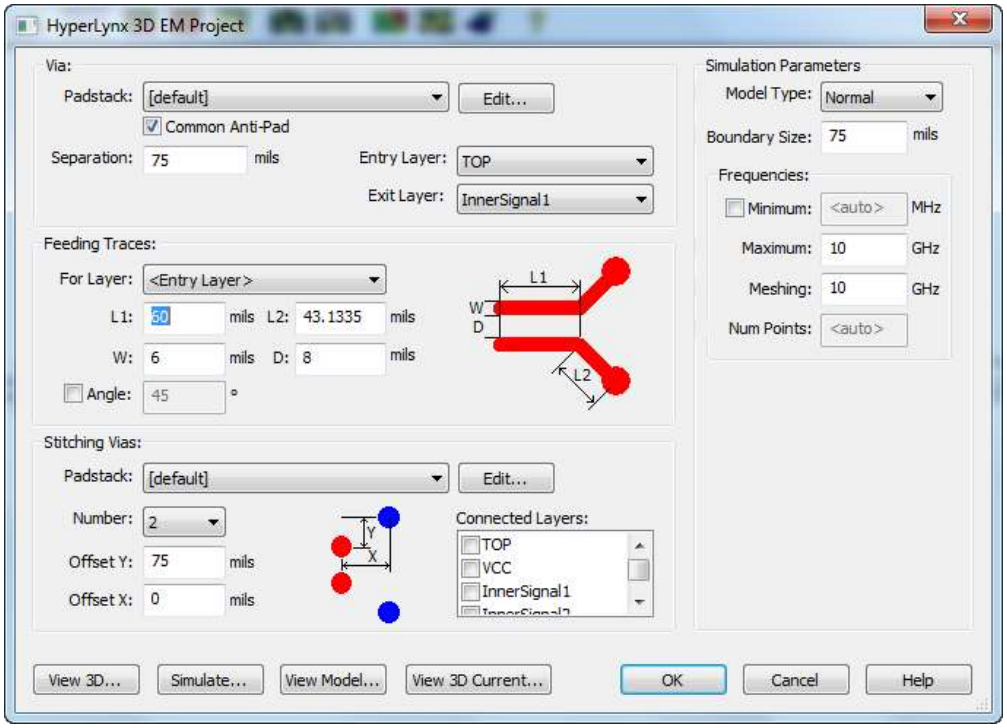


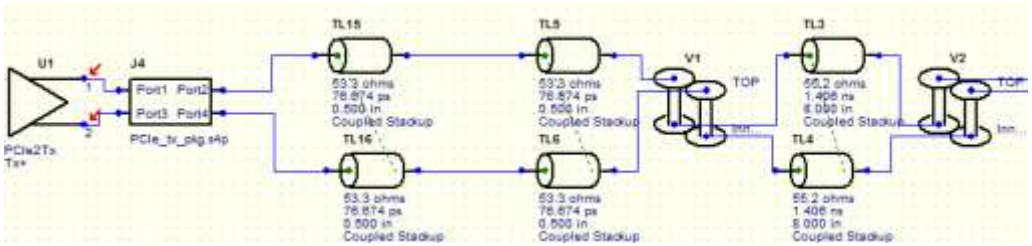




SI Enhancements

8.2





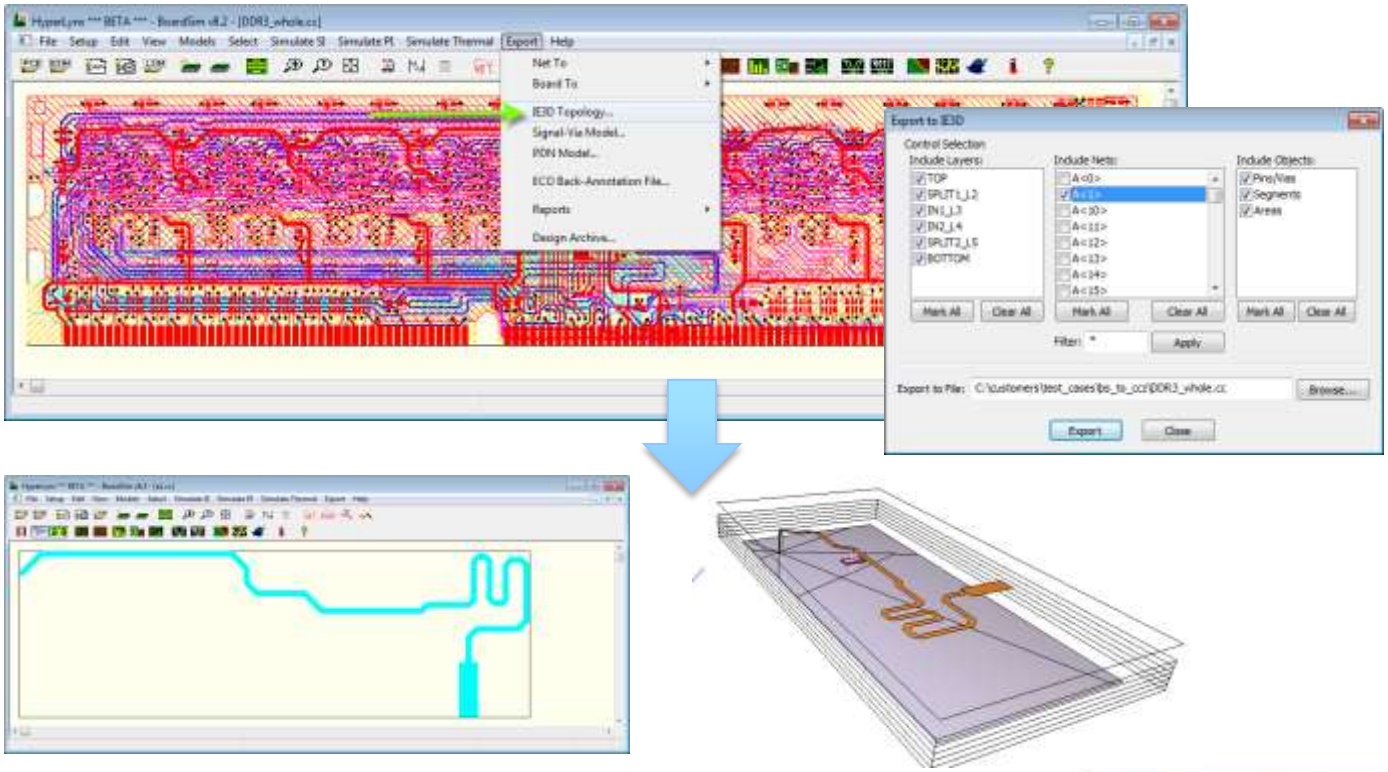
- 3D via modeling
  - Differential and single ended 3D via models
  - 0, 2, or 4 stitching vias supported
  - Entry trace automatically removed from adjoining transmission line segments in schematic
  - All via geometry information directly driven from standard HL via visualizer
  - 3D viewing of via structure

SI Enhancements

8.2

BoardSim export to HyperLynx 3D EM

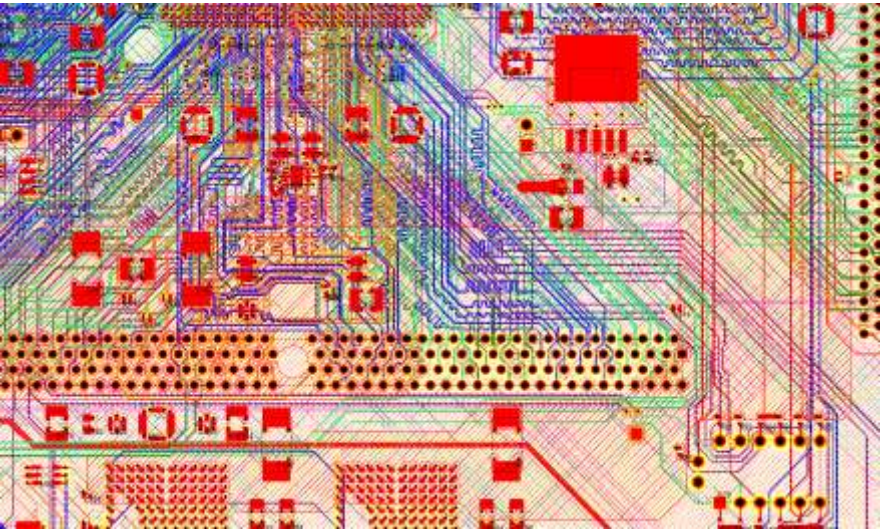
- Allows users to select small areas of a design for export to HyperLynx 3D EM for detailed 3D modeling

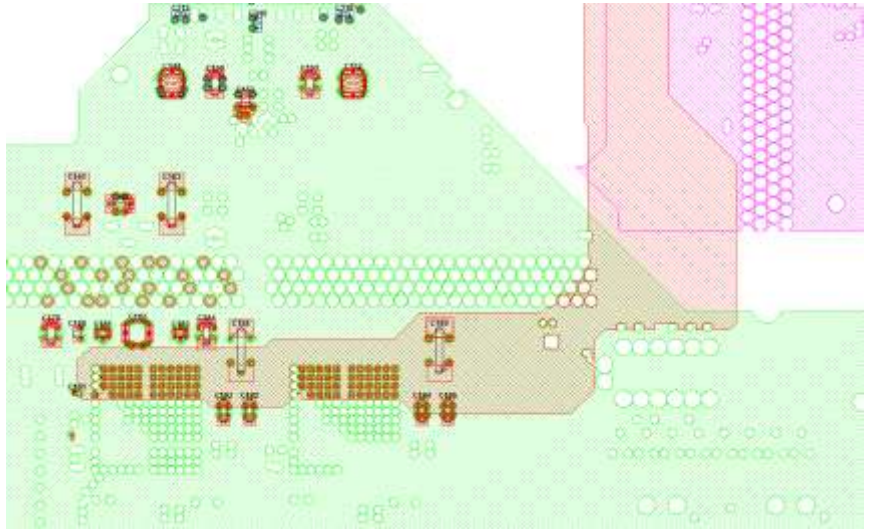


PI Enhancements

8.2

- PDN editor “net awareness”
  - Requested by CSD as one of the“most-critical-to-fix-problems” in v8.2

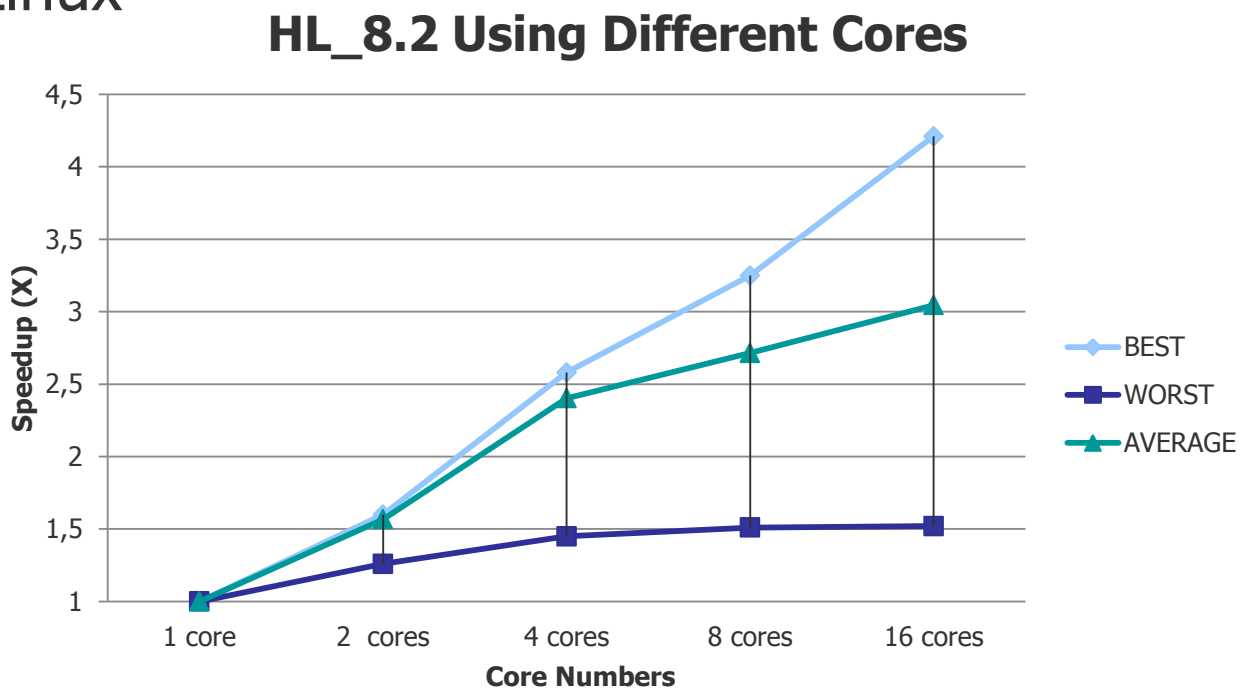




PI Enhancements

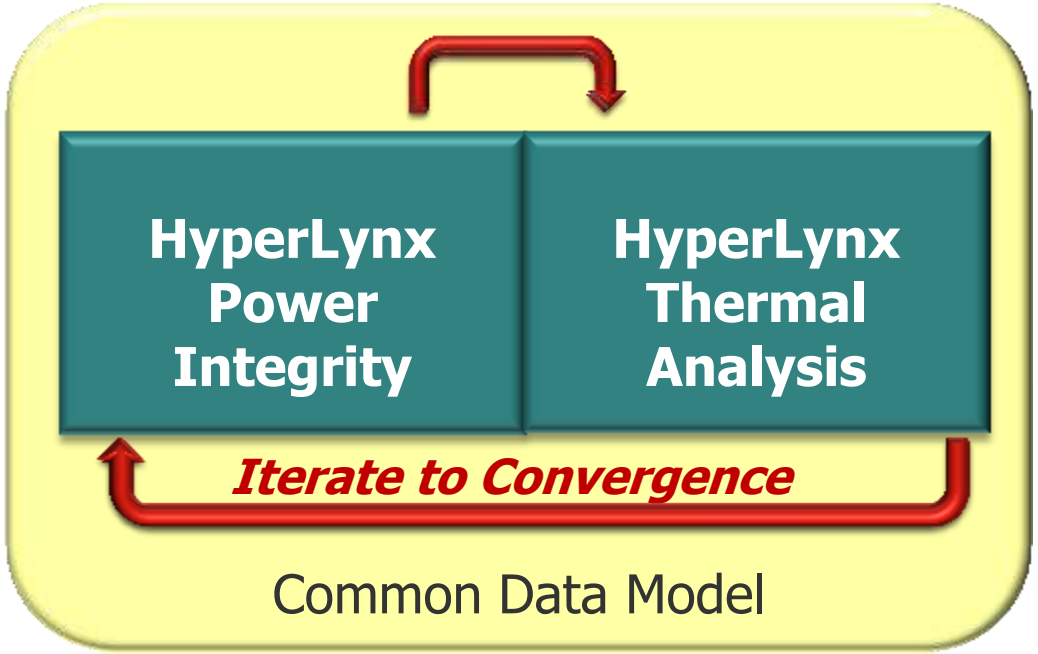
8.2

- Multi-core simulation support
  - Up to 16 additional cores can be used on a single machine
- Intel math libraries
- 64-bit Linux



Integrating HyperLynx Thermal and Power Integrity

- More accurate IR drop analysis
  - Capture increased resistivity due to heating
- More accurate PCB thermal analysis
  - Incorporate heating due to power current density



Accurate PDN DC drops & current densities

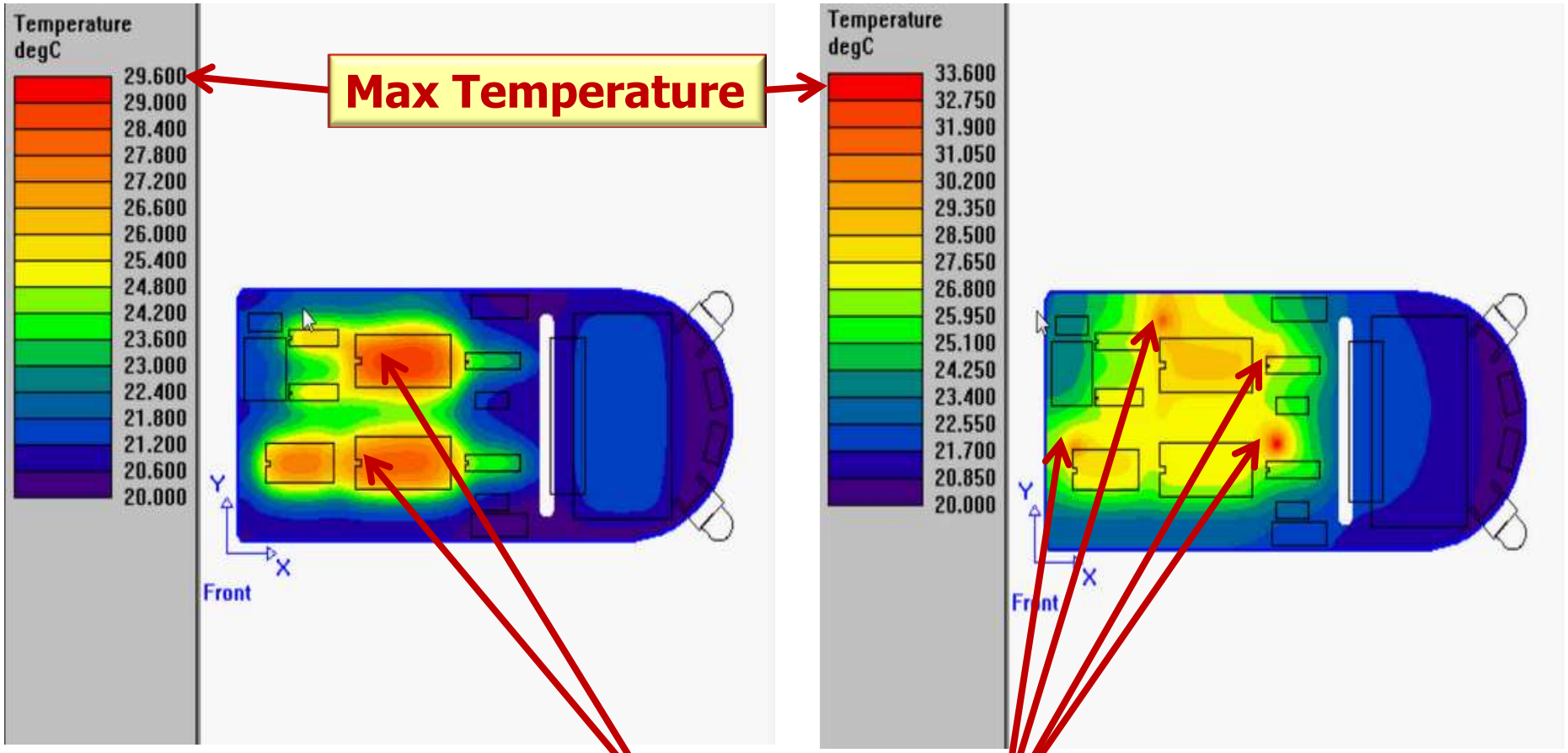
Accurate resistivity & signal integrity

Accurate PCB thermal analysis

Integrating Power Integrity and Thermal Gives More Accurate Results

Standalone Thermal Analysis

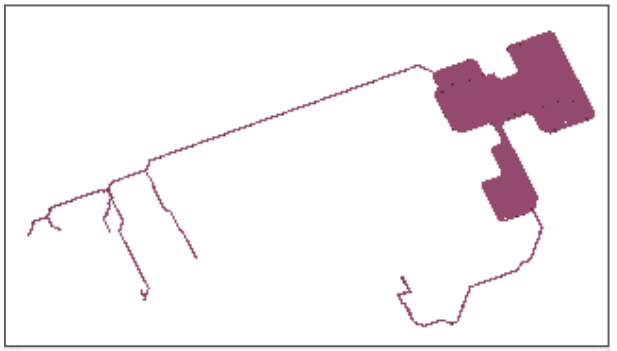
Thermal with Current Density

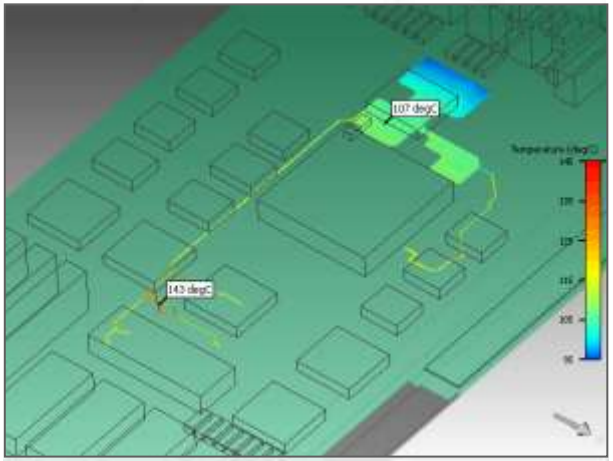


PI/Thermal Enhancements

8.2

- Power integrity/FloTHERM interface
  - Exports a detailed description of dissipated power distribution
  - Information will be imported into FloTHERM
    - Provides a more complete 3D PCB model
  - Resulting temperature predictions will then be available to judge the risk of thermo-mechanical related trace/net failure
    - Including effects such as local heating effects of high powered actives, heat loss due to air convection etc.





HyperLynx DRC

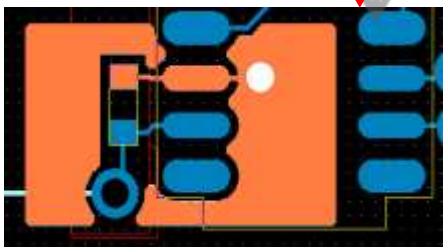
6.0

- **D**esign **R**ule **C**hecks
  - Automates design checks, eliminating errors from manual inspection
  - Reduces days of manual design checks to a few hours
- Includes built-in rules
  - Design rule checks for EMI, SI, PI
    - Items not quickly/easily simulated
- Allows for rule customization
  - Easily access database objects through automation
  - Advanced geometric operations
  - Script writing/debugging environment
- HyperLynx DRC 6.0 release plan
  - Release in summer 2012

HyperLynx DRC – Fully Customizable

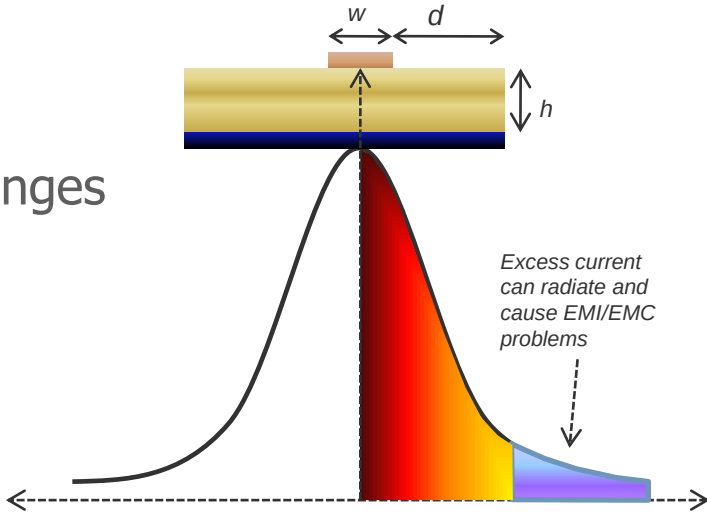
- Subject matter experts create custom rules
  - Distribute to multiple users/sites
  - Uniform design reviews across organization
- Complete DRC creation environment
  - Supports VBScript, JavaScript
  - Script debugger
  - Extensive documentation on AOMs, DRC writing guidelines

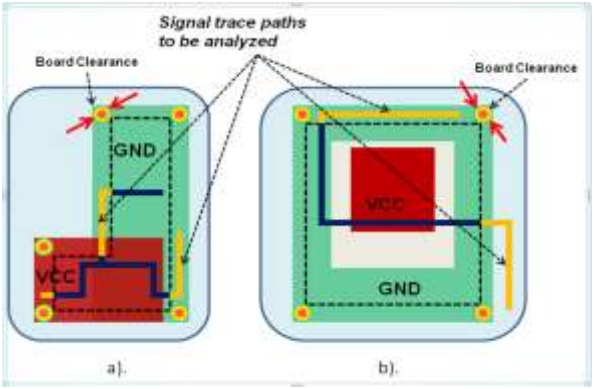
- Design access through Automation Object Models (AOM)
  - Allows for powerful, flexible custom rules
  - Can develop any kind of rule imaginable
- Built-in rules included
  - Can be used as examples



HyperLynx DRC Built-in DRCs

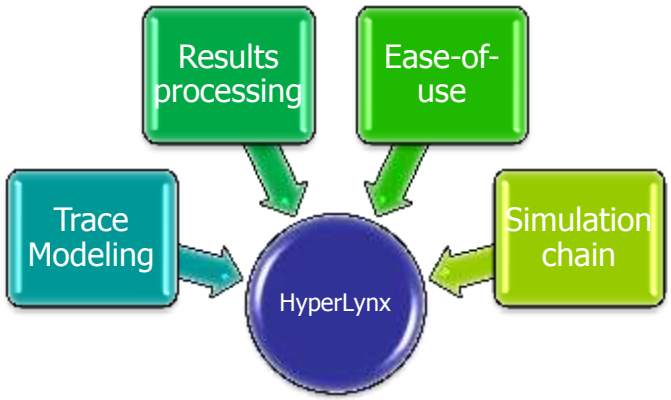
- 22 built-in DRCs included
- EMI examples
  - Traces crossing splits, reference plane changes
  - Nets near edge, coupling to I/O nets
- SI examples
  - Long nets (SI risk), termination check
  - Number of vias, shielding
- PI examples
  - Power net width, decoupling cap proximity
- Future plans include
  - Schematic DRCs
  - Mixed schematic/layout DRCs
  - Integrated Field Solver





HyperLynx 9.0

- Deliver one product with Mentor's best technology
  - Re-use technology wherever possible
- Integrate existing compelling technologies within HyperLynx
  - Improved trace modeling
  - Results management
  - Faster simulator
- DC drop results viewing improvements
- Pre-layout DDRx
- Release timeline
  - Alpha testing in select accounts since December 2011
  - Open Beta started summer 2012
  - Release in Q4 2012



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