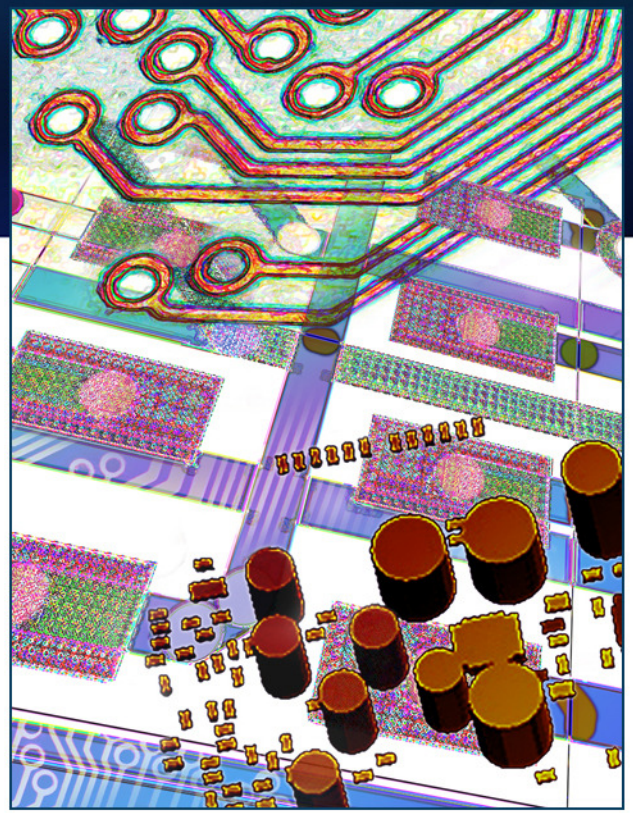


HyperLynx Products

Steve Gascoigne

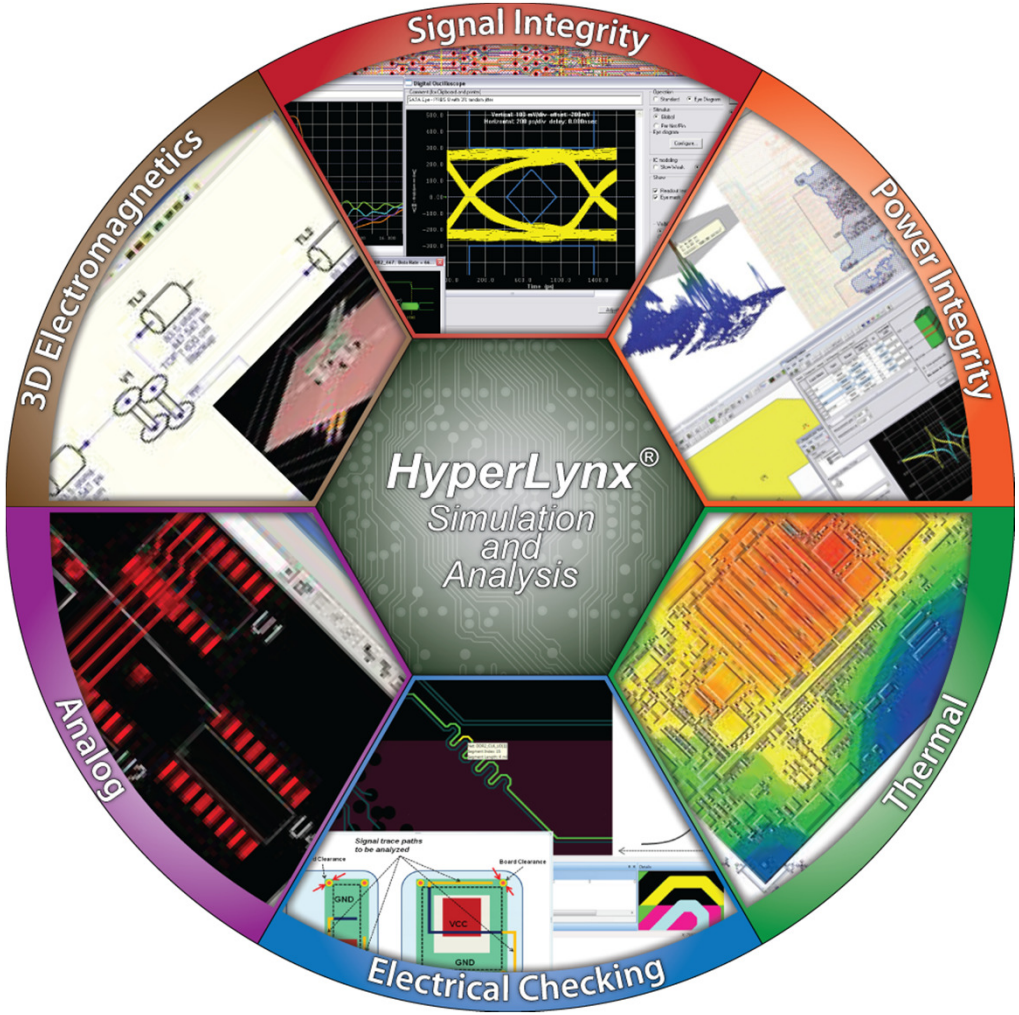
Application Engineer Consultant

Focus Products Organization

Mentor Graphics®

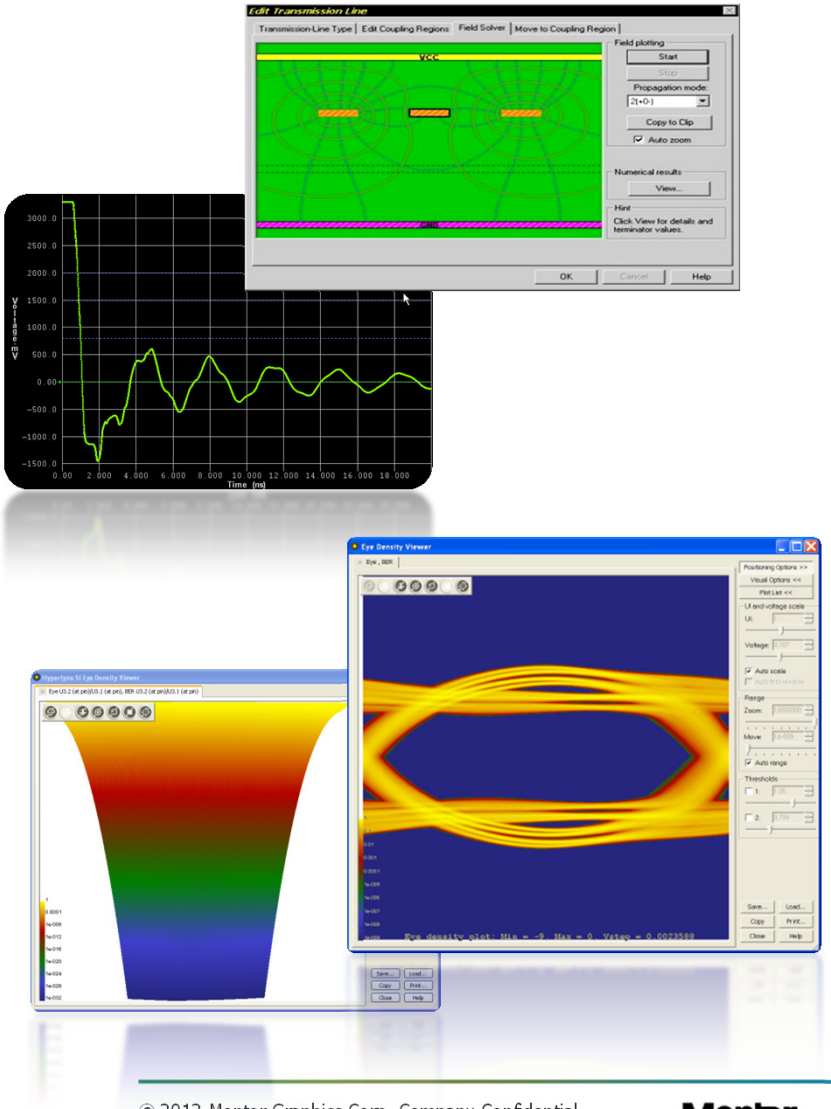
A Complete Analysis Solution

- Address multiple design areas through virtual prototyping
- Integrated technologies to accelerate adoption
- Ease-of-use enables ALL engineers to perform analysis
  - PCB designers thru SI/PI specialists



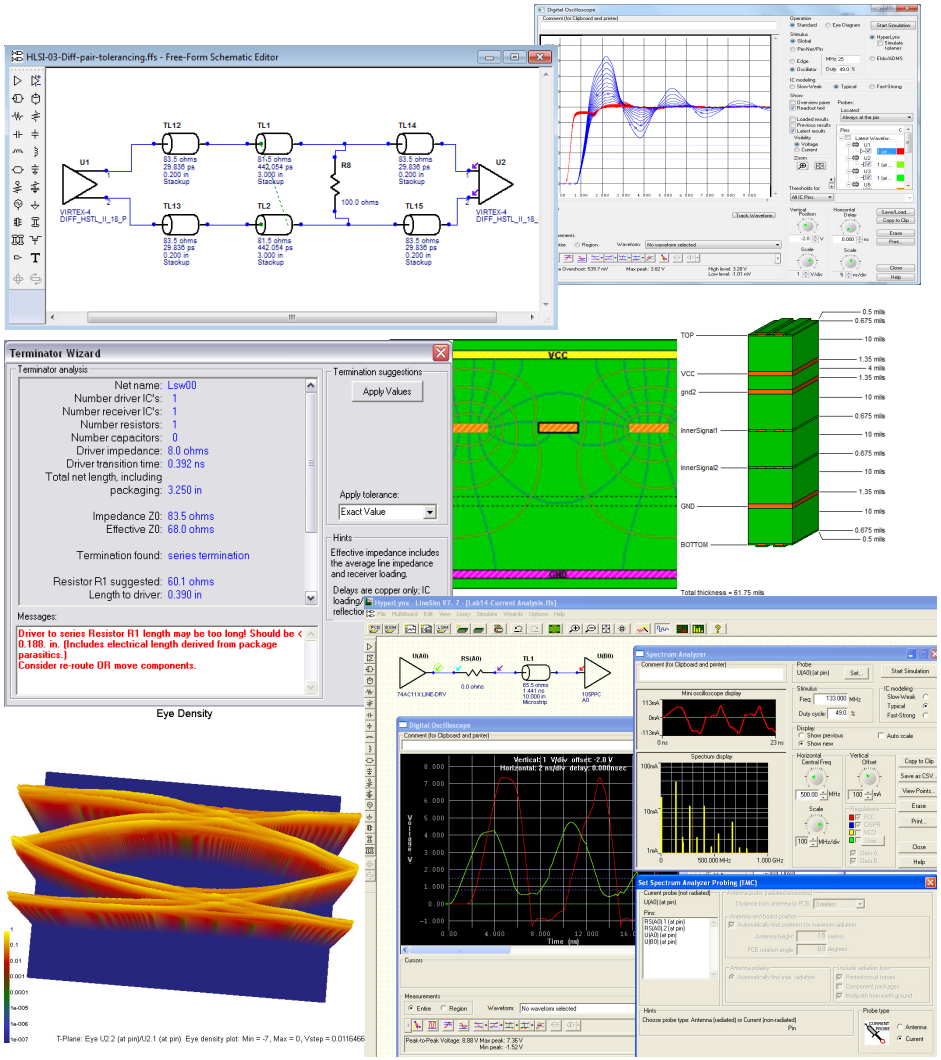
Signal Integrity Concerns

- Traditional signal integrity
  - Crosstalk, overshoot, timing, impedance
- DDRx design
  - Timing, ODT selection
- Multi-gigabit SerDes technologies
  - Loss management, via design, length matching, impedance discontinuities



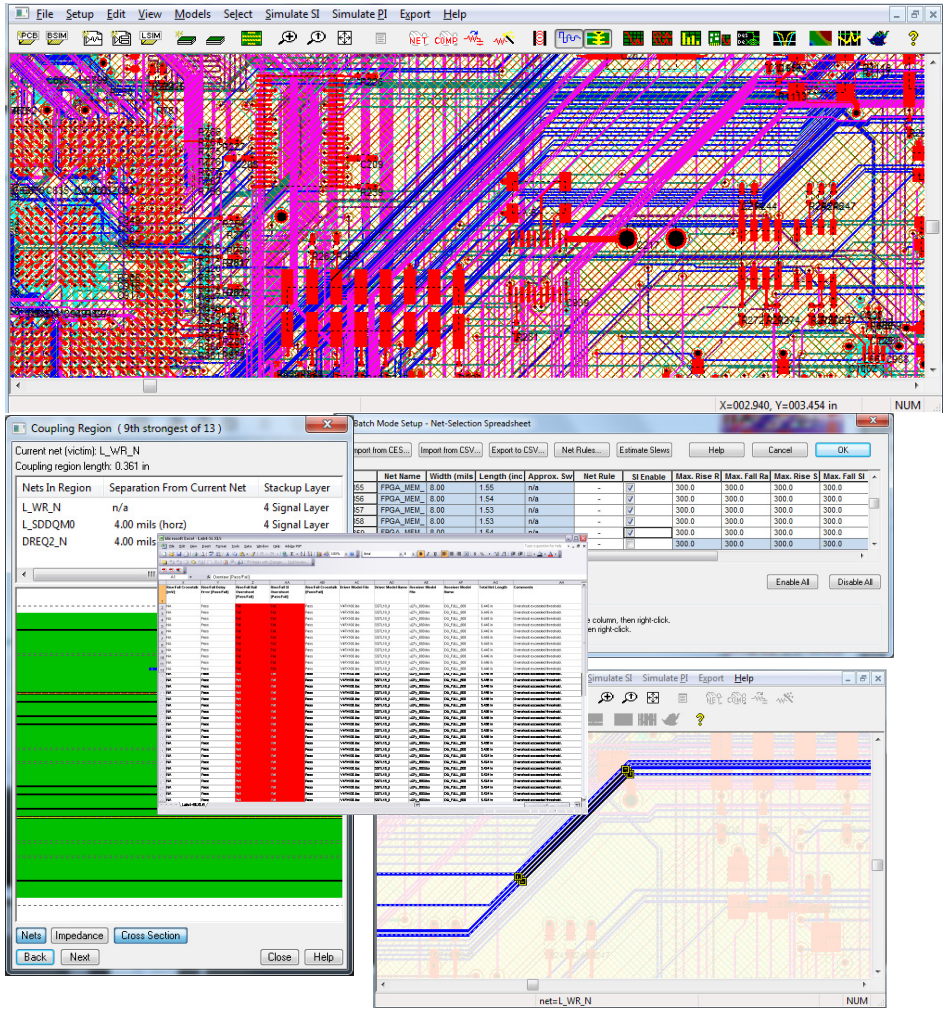
HyperLynx: LineSim SI

- Industry-renowned ease of use
- Accurate modeling of trace impedance, coupling & frequency-dependent losses
- Terminator wizard recommends optimal termination strategies
- Identify SI issues, perform crosstalk analysis & parametric sweeps
- Stackup planning
- Industry-leading for SERDES, including fast eye diagram analysis, S-parameter simulation, and BER prediction
- Advanced via modeling
- Provides an early look at EMC
- Integration with the CES



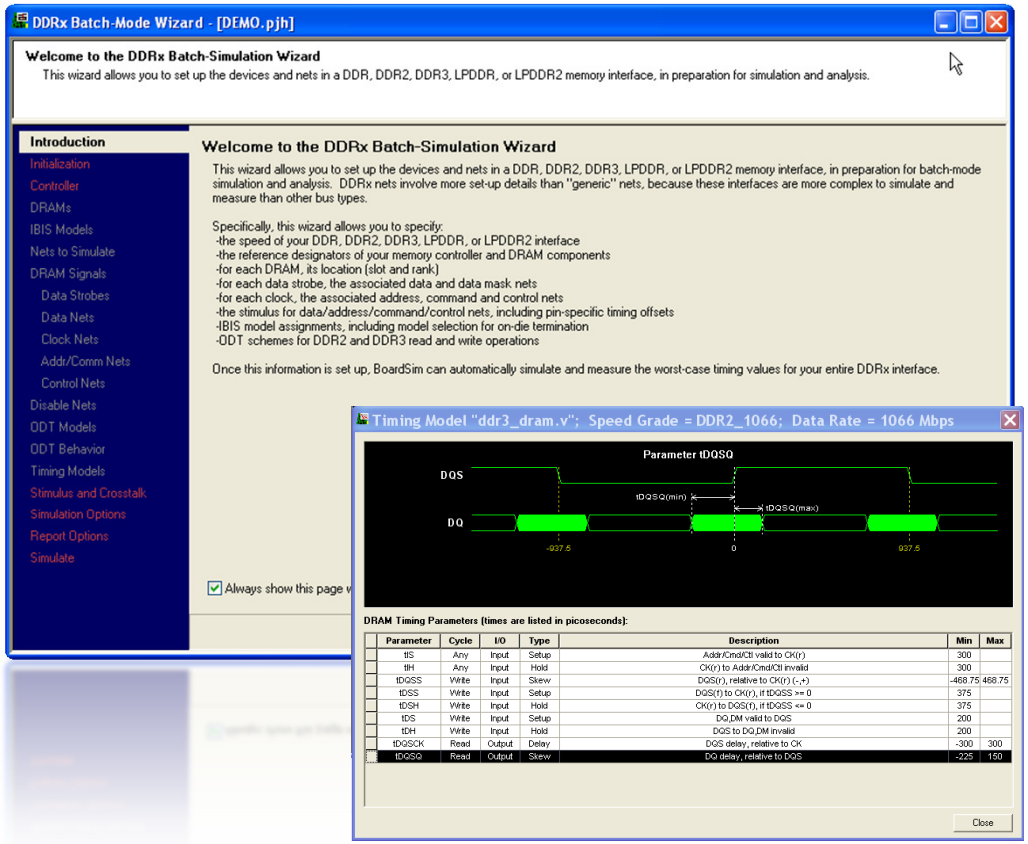
HyperLynx: BoardSim SI

- Simulate post-routed data from Expedition Layout
- Run interactive simulations on individuals nets
- Run a comprehensive batch simulation on many nets at once
- Parametric sweeps
- Verify DDR/2/3 bus structures (single and multi-board setups)
- Crosstalk analysis
- Advanced Timing Analysis
- Interactive EMC Analysis
- Run SERDES Fast-eye analysis
- Run IBIS-AMI channel analysis



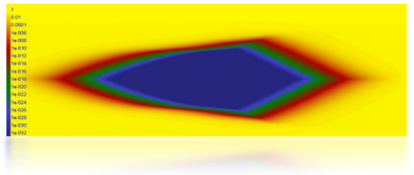
HyperLynx DDRx Simulation

- Validate LPDDR and DDRx timing and SI designs
  - Analyze timing for both address and data buses
  - Measurements for clock to strobe skew
  - Measure timing and SI on all signal edges
  - Advanced crosstalk simulation
- Analysis is simplified through an interview process

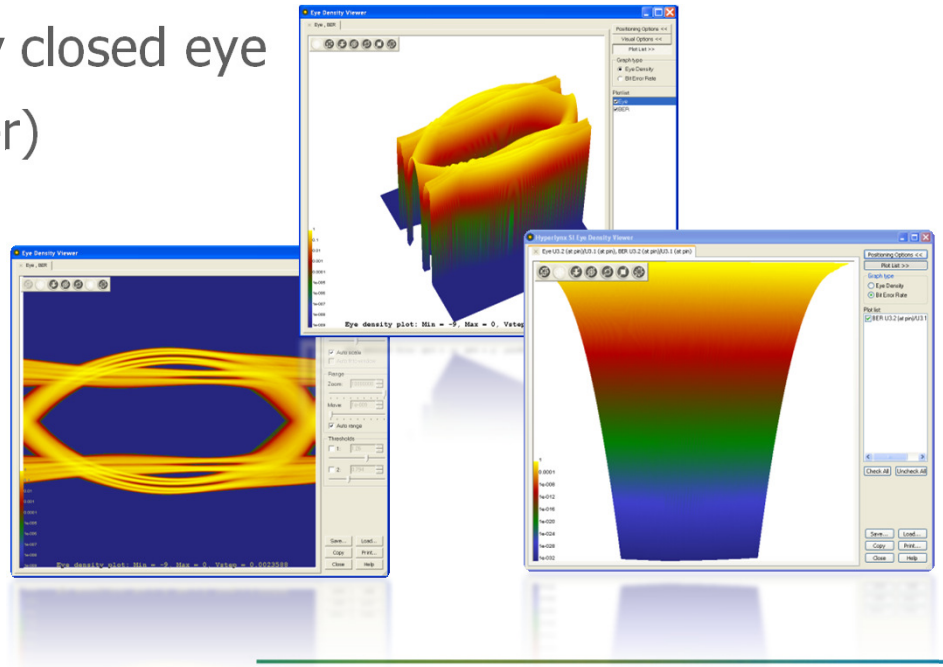


Multi-Gigabit Channel Analysis

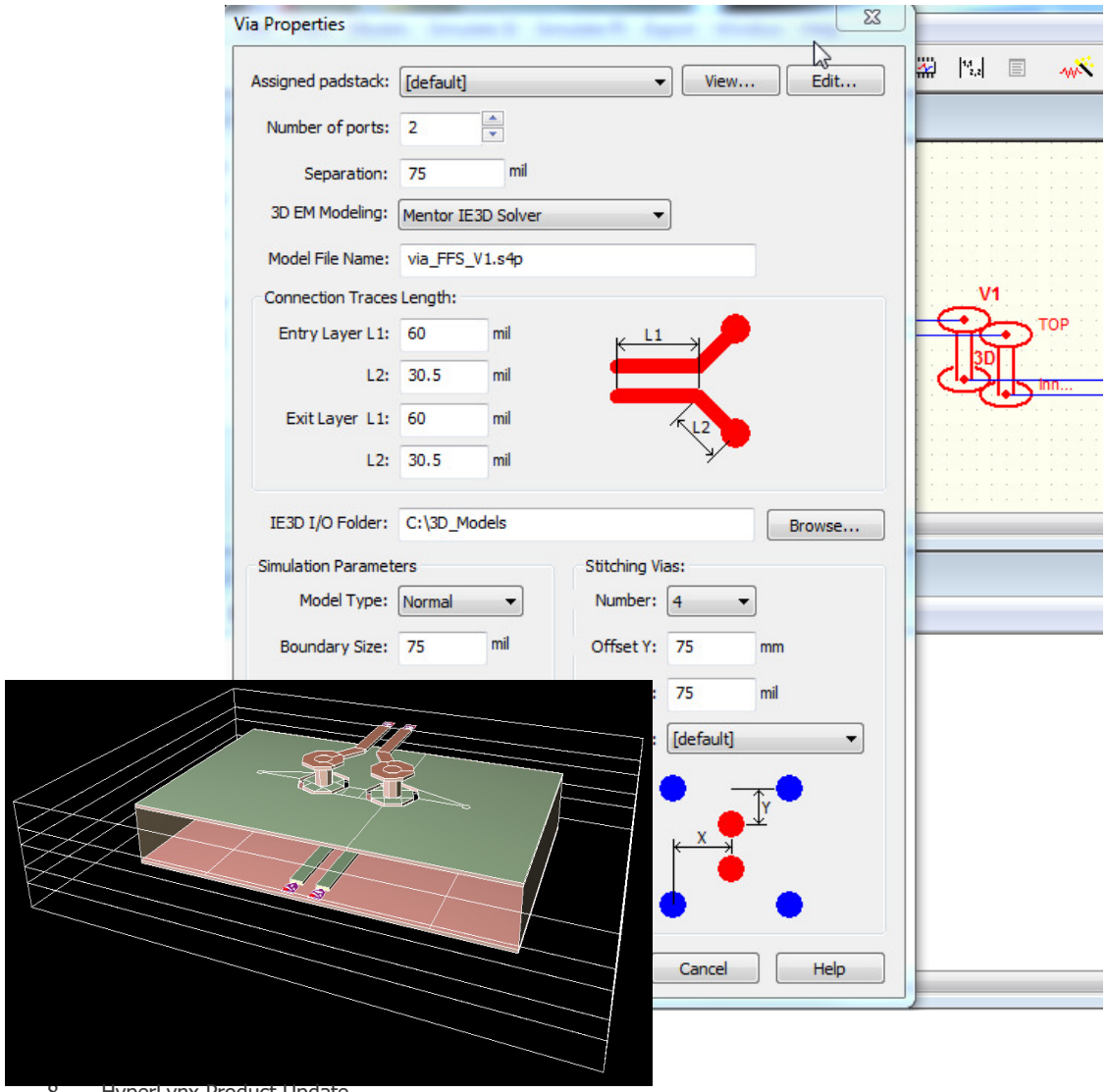
- Fast time domain and statistical analysis
  - Simulate millions to billions of bits for accurate BER prediction



- Generate the channels worst case bit sequence
  - PRBS or 8B/10B protocol dependant
  - Always produces a maximally closed eye
  - Bounds Dj (deterministic jitter)
- Validate BER
  - Eye density plots
  - BER plots
- Support for IBIS-AMI, SPICE, S-Parameters



Full-Wave 3D Via Modeling



- Some designs require more accurate via models
  - Can contribute significant loss at higher frequencies
- Need the ability to accurately tune the via design
  - Separation, stitching, entry angle, etc.
- 3D simulation provides highly accurate models up to 100+ Gbps frequencies

3D Full-Wave EM Modeling

HyperLynx 3D EM

- Based on IE3D technology
  - Fastest, highest-capacity, full 3D EM simulation in the market
- NEW product for Mentor Graphics
  - Zeland Software, Inc. acquired February 2010
- Creates high-frequency parasitic models needed for circuit simulation
  - Frequency-dependent parasitic extraction of metallic structures – "s-parameter models"
- Highly respected for EM design & verification
  - Over 1600 customers
  - Long history (since 1992) of production proven use

$$\oint_C \vec{E} \bullet d\vec{S} = \frac{q}{\varepsilon_0 \varepsilon_r} = \Phi_E$$

$$\oint_C \vec{B} \bullet d\vec{S} = 0 \quad \oint_C \vec{B} \bullet d\vec{S} = \Phi_B$$

$$\oint \vec{E} \bullet d\vec{l} = -\mu_0 \mu_r \frac{d\Phi_B}{dt}$$

$$\oint \vec{B} \bullet d\vec{l} = \mu_0 \mu_r \left(\varepsilon_0 \varepsilon_r \frac{d\Phi_E}{dt} + i \right)$$

Employs a Unique 3D Integral Equation Method to Solve Maxwell's Equation Governing Electrical Behavior of Metallic Structures

Application of HyperLynx 3D EM

EM Simulation is Used in All High-Frequency Design Applications

- Wireless
  - Cell phone, routers, Bluetooth, GPS, LTE, wimax (802.16)
  - Antenna and antenna arrays
  - RFID/zigbee tag design
- Hi speed digital
  - 10G/40G+ internet, Fibrechannel, XAUI, PCIE, Infiniband
  - On-chip SerDes, package
  - DDR2/DDR3 memory I/F channel
- Military/aerospace
  - Secure communications/network
  - Large phase array/imaging antenna
  - Compact multi-band antenna
  - Materials research

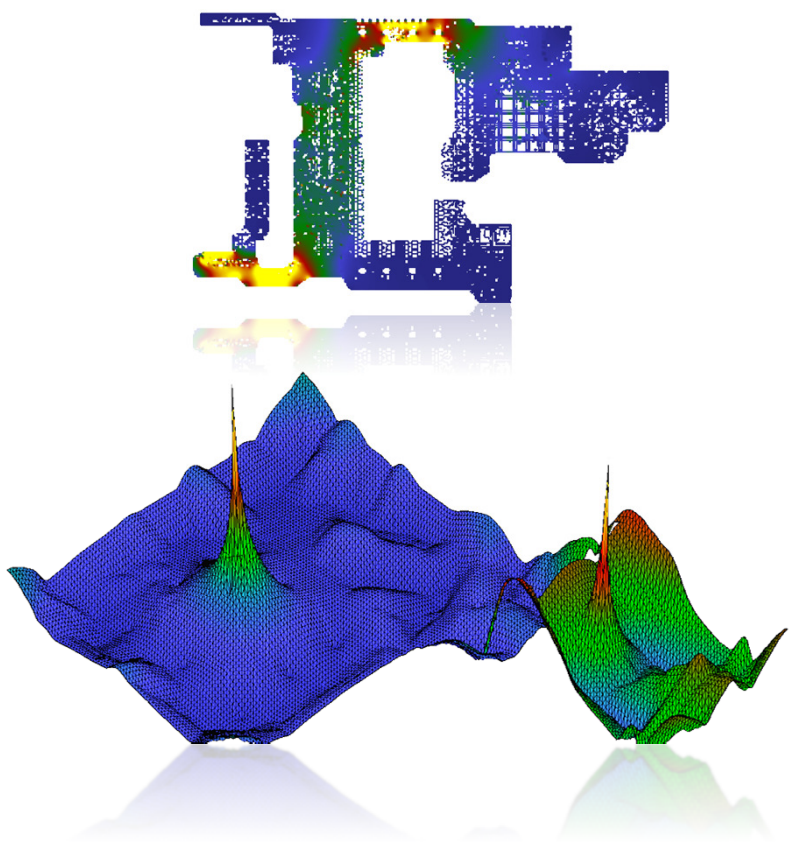
HyperLynx 3D EM Value

Fastest commercial 3D EM simulator
Has the largest design capacity
Accuracy matches measurement
Packaged for widespread deployment

- Fastest EM design closure
  - More simulations/hour accelerates design convergence
  - Higher capacities alleviate need to manually partition design
- Lower EM design costs
  - Unique, scalable distributed EM simulation
  - Replace less-capable, more-expensive competitive alternatives
  - Reliable, predictable results reduces risks of costly design iterations
- Improve design quality - minimize EM design re-spins
  - Higher simulation coverage helps ensure nothing was missed
  - Higher capacity – detect hard-to-find EM design flaws prior to prototype
  - Reliable, predictable results increases designer confidence

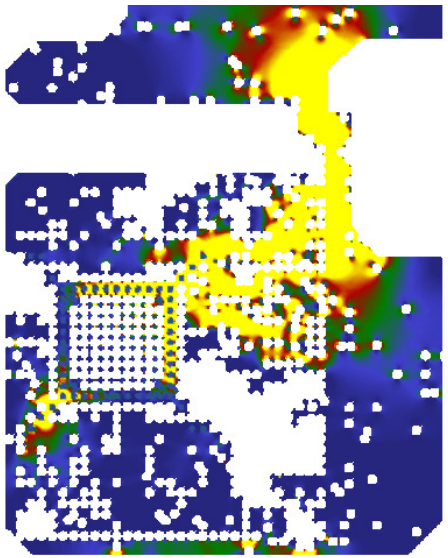
Power Integrity Analysis

- DC drop analysis
  - Identify excessive voltage drop and high current densities
  - Determine if there is enough copper & stitching vias
  - Batch analysis of all power nets
- AC power plane analysis
  - Optimize capacitor selection and mounting
  - Verify power supply impedance at IC power pins
  - Analyze voltage ripple on power nets



IR Drop Design Issues

- Common problems:
  - Not enough voltage getting to ICs from power supplies
    - Leads to IC malfunction
  - High current densities in voltage island neck-downs and vias
    - Leads to dielectric or via breakdown and board failure

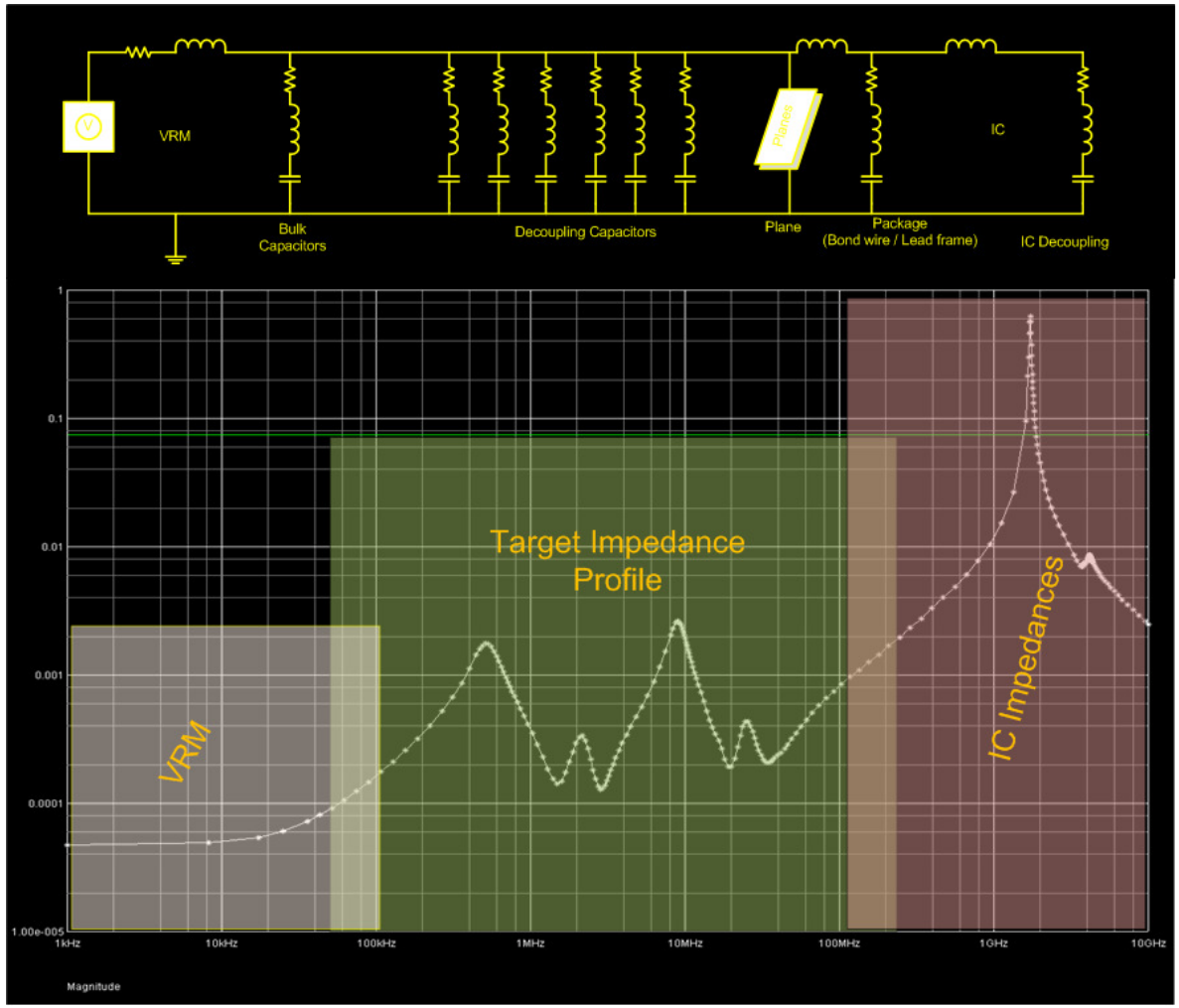


High Current Density

Excessive Voltage Drop

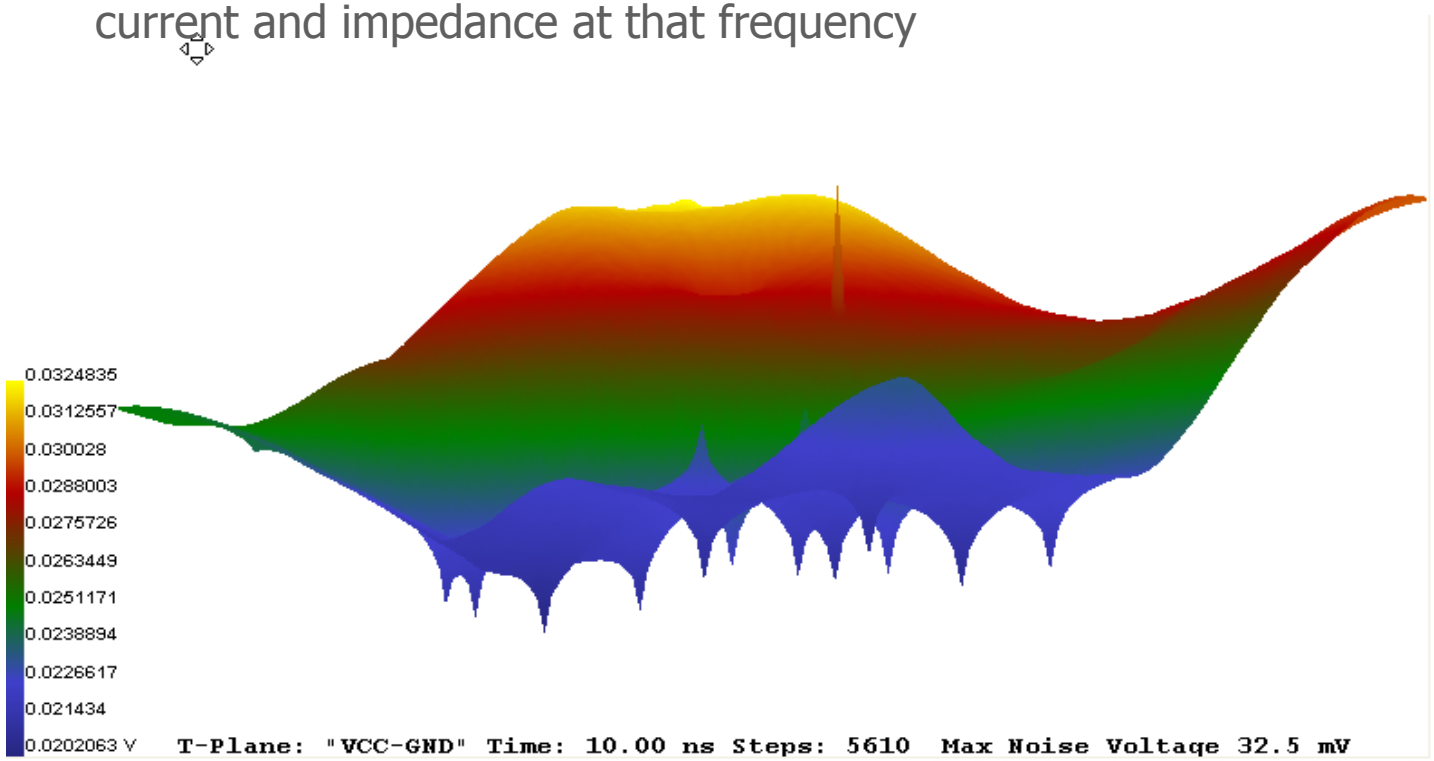
Decoupling Design

- Develop decoupling methodologies to
  - Properly design stackup for power
  - Design capacitor mounting structures
  - Make intelligent capacitor selections
- Goal = Achieve IC Target Impedances for power
  - Set by voltage ripple requirements



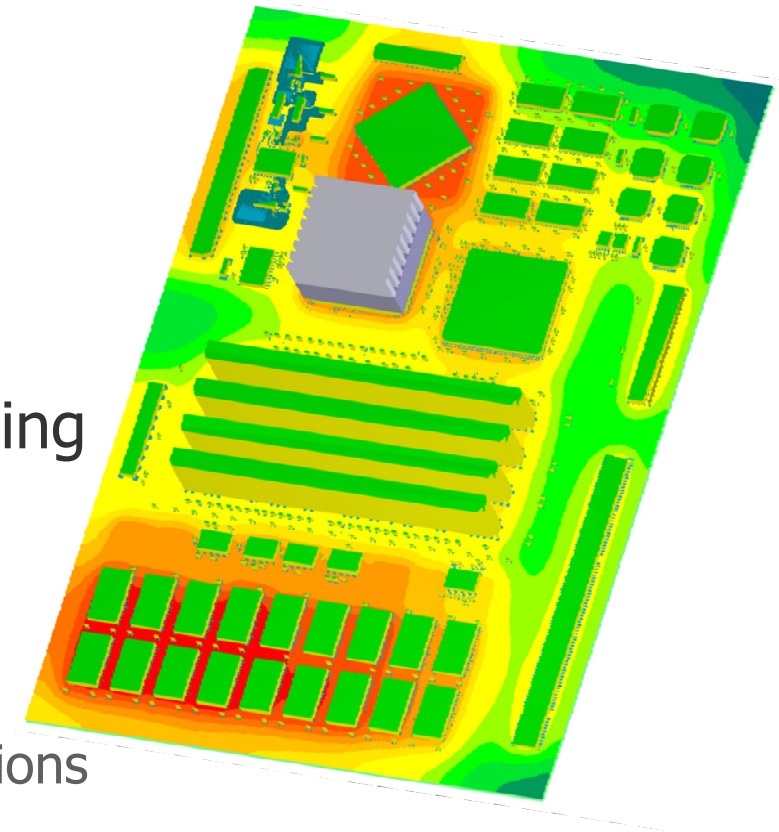
Plane Noise Analysis

- HyperLynx Plane Noise can help identify voltage ripple exceeding IC power pin specifications
- Plane noise is a result of target impedance and switching currents
  - (V=I*R)
  - Amount of voltage noise is dependant on edge rate (frequency) of current and impedance at that frequency



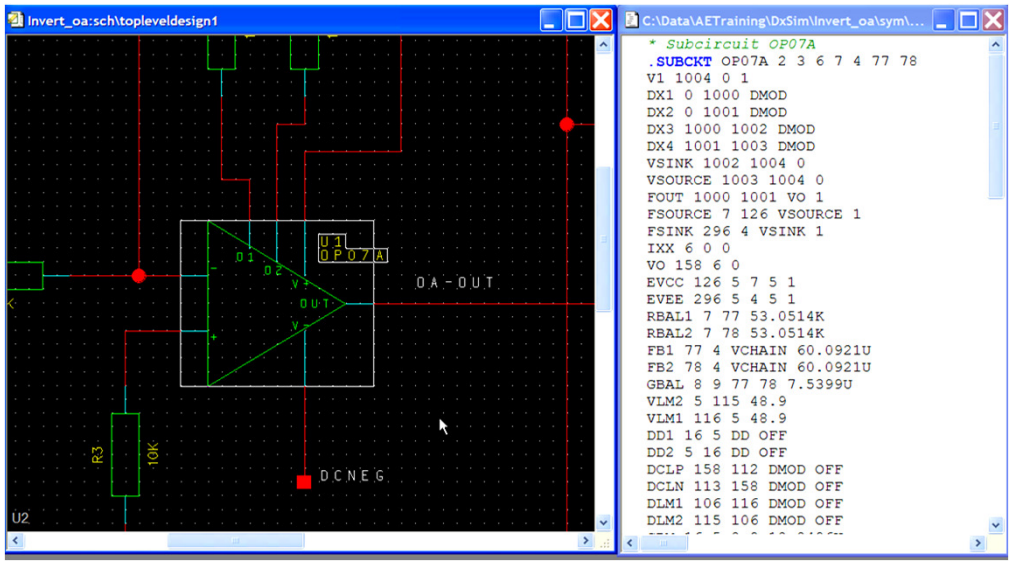
Thermal Analysis

- Allows engineers and PCB designers to identify component and PCB hot spots
- What-if analysis on
  - Component placement
  - Stackup design
  - Mechanical cooling techniques
- Quick and accurate analysis including
  - All PCB copper
  - Packages, Pins, vias, screws, etc
  - Environment including enclosure
  - Package to Board, Pin to Board junctions
  - Heat sinks and Airflow



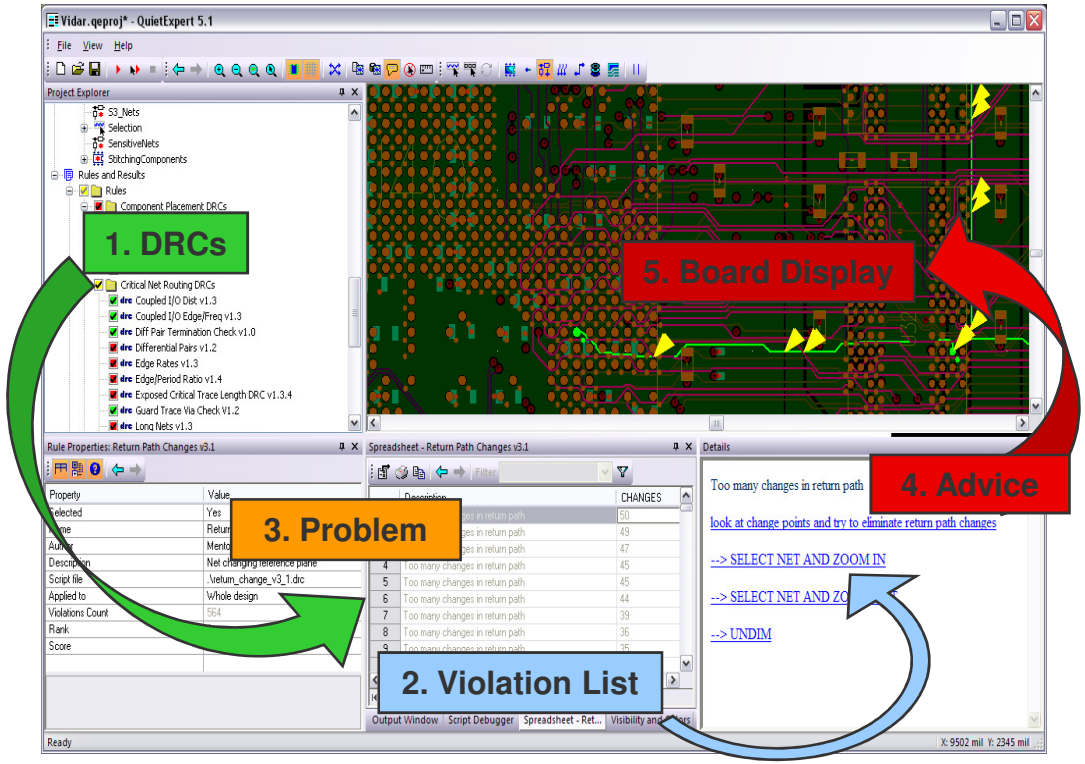
Analog Simulation

- Scalable simulation solution built on DxDesigner
- Analog and full mixed signal simulation capability
  - Support for analog and digital primitives
  - Standard language support
    - VHDL, VHDL-AMS, Spice, & Verilog-A
  - Power ADMS and Eldo simulation kernels
- Full featured waveform viewing with EZWave
  - Including complex waveform calculations



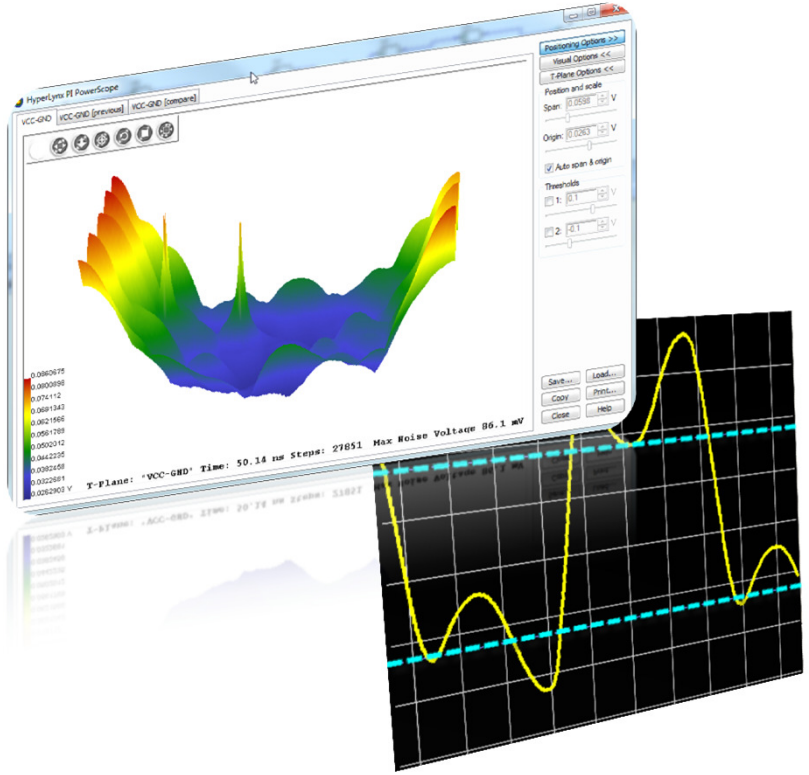
EMI / PCB Verification

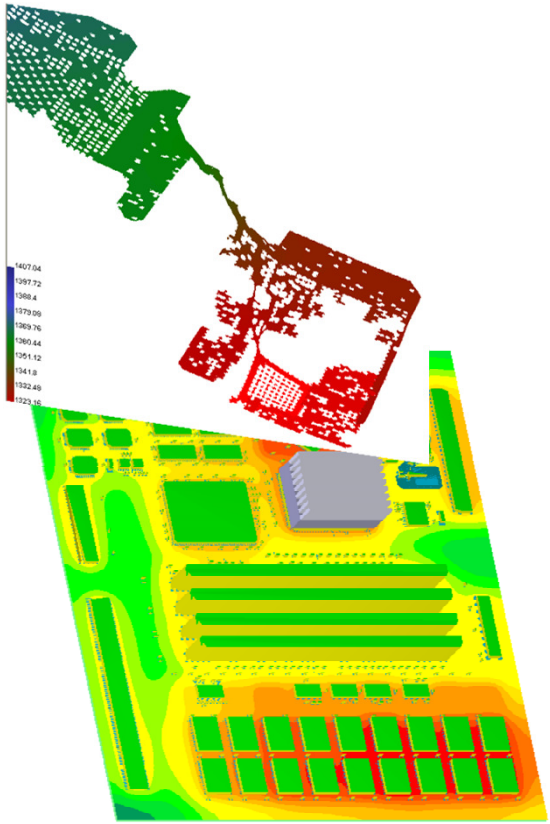
- PCB Design Validation
  - Rules-based verification of the PCB
  - Finds problems before building prototypes
  - Create custom design rules to identify **your** common problems
- Automates the design review process
  - Enables consistency
  - Minimizes human error
  - Reduces design review time investment



Crossing Domains

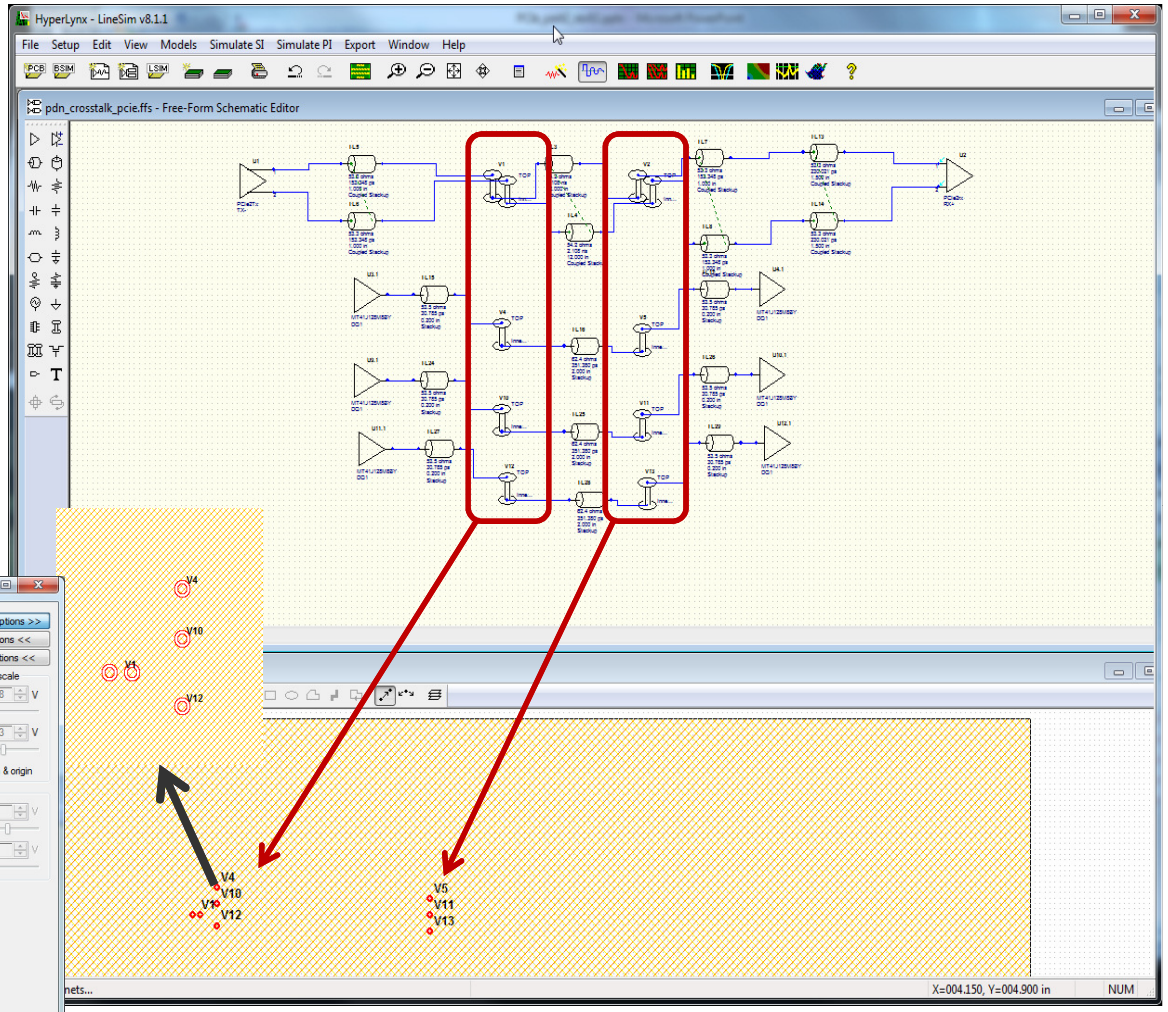
- Sometimes independent analysis addresses only part of the issue
- Integrated Analysis flow allows for simulation across domains

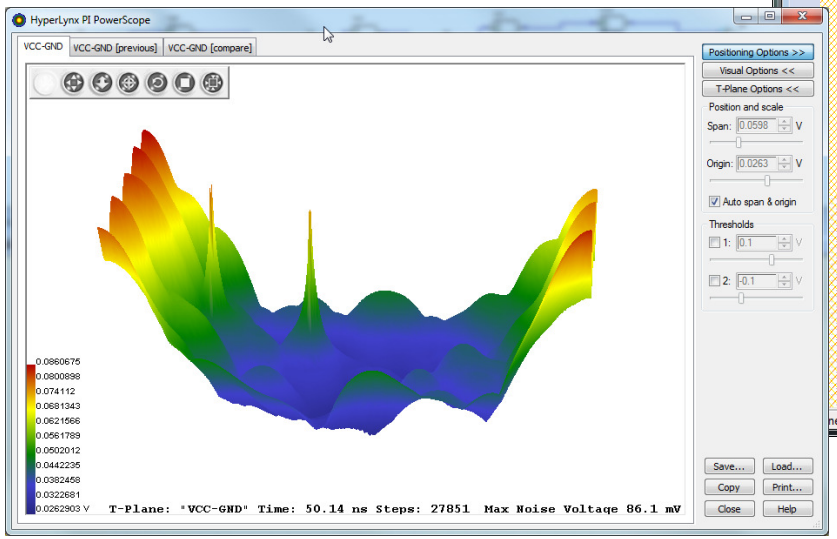




Simulating Via-to-Via Crosstalk

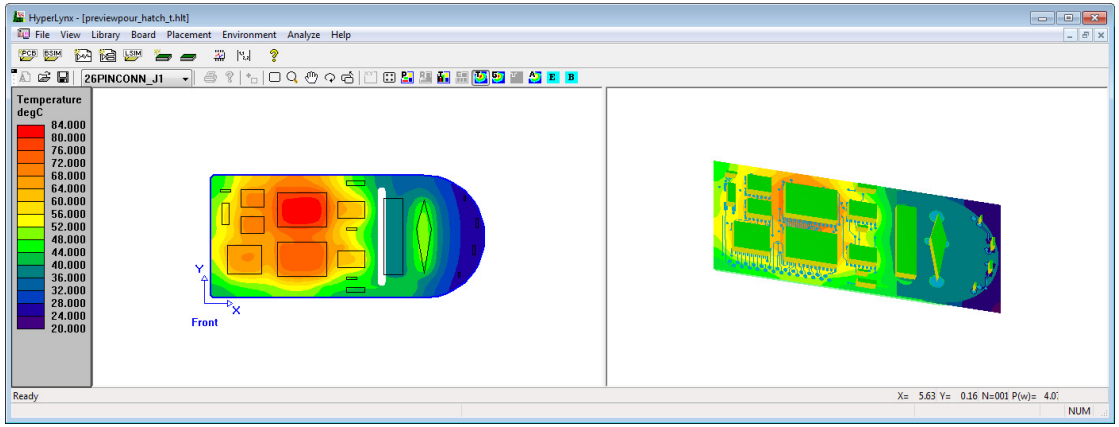
- Mixed signal and power integrity simulation
  - Via crosstalk through power planes





PI/Thermal Co-Simulation

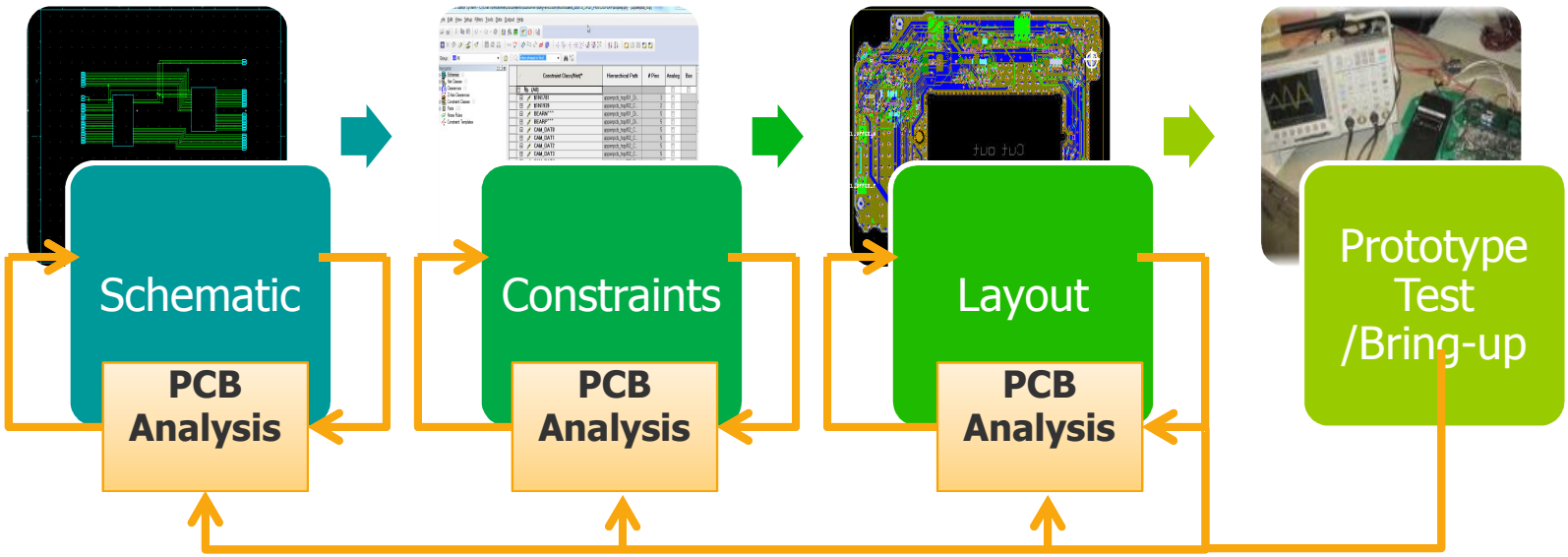
- HyperLynx Thermal within the existing HyperLynx SI and PI environment
- Co-Simulation capabilities between PI and Thermal
  - Power Integrity engine (DC drop) simulates power nets provides power density "map" to thermal solver
  - Thermal solver runs thermal analysis with component power dissipation and results from PI simulation
  - System runs several iterations of above process with PI simulator using updated resistances(based on temp) until convergence



Analysis is Core to the Design Process

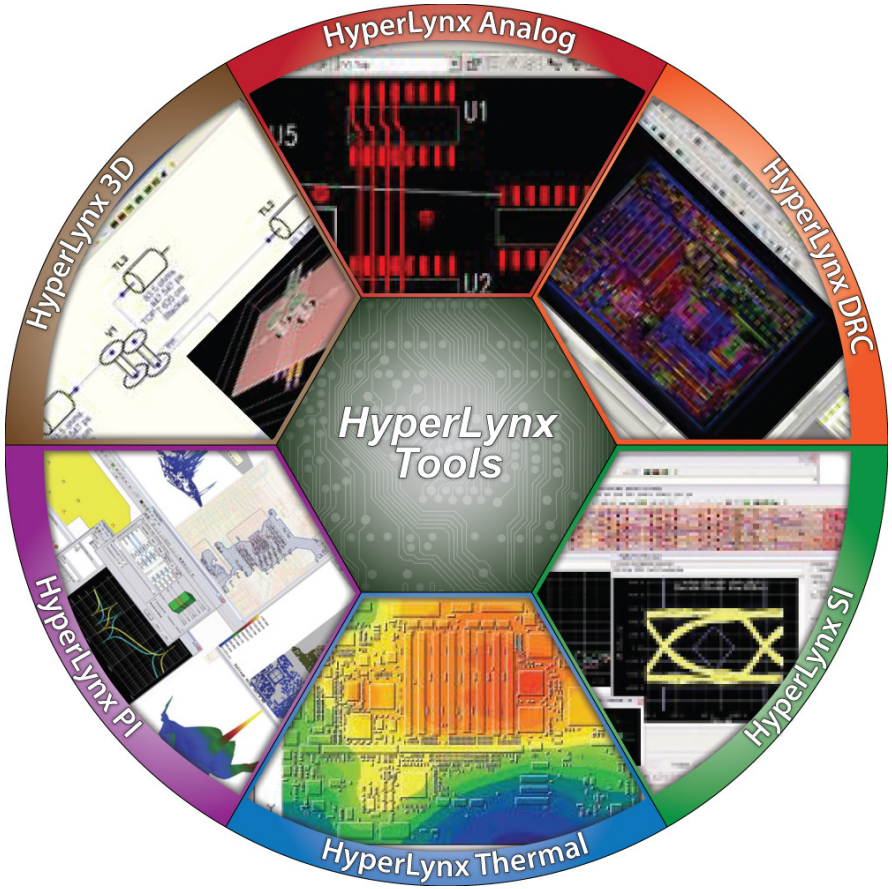
- PCB design is more than schematic and layout
  - We know designs are becoming more complex
- To meet reliability and time-to-market
  - Project engineers must do PCB Analysis

"HyperLynx is now mandated as part of our PCB design process."
- SEAKR Engineering



HyperLynx Analysis Environment

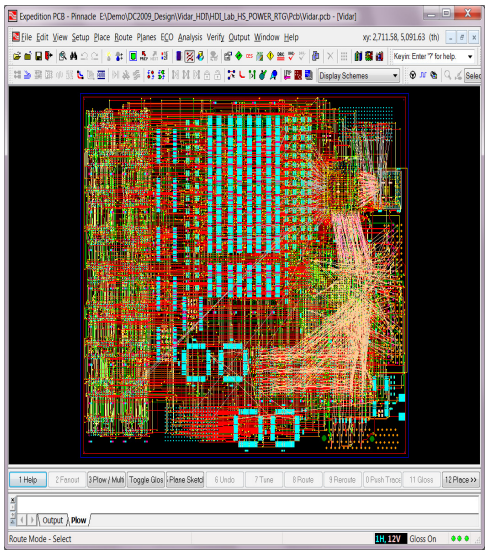
- Comprehensive suite of analysis technologies
  - — Reduce design cycle time
    - – Develop constraints for "first time right" design
  - — Improve design reliability
    - – Validate design intent before prototyping
  - — Verification in multiple domains
    - – Accurate & fast time-to-results
  - — HyperLynx enables ALL engineers to drive analysis

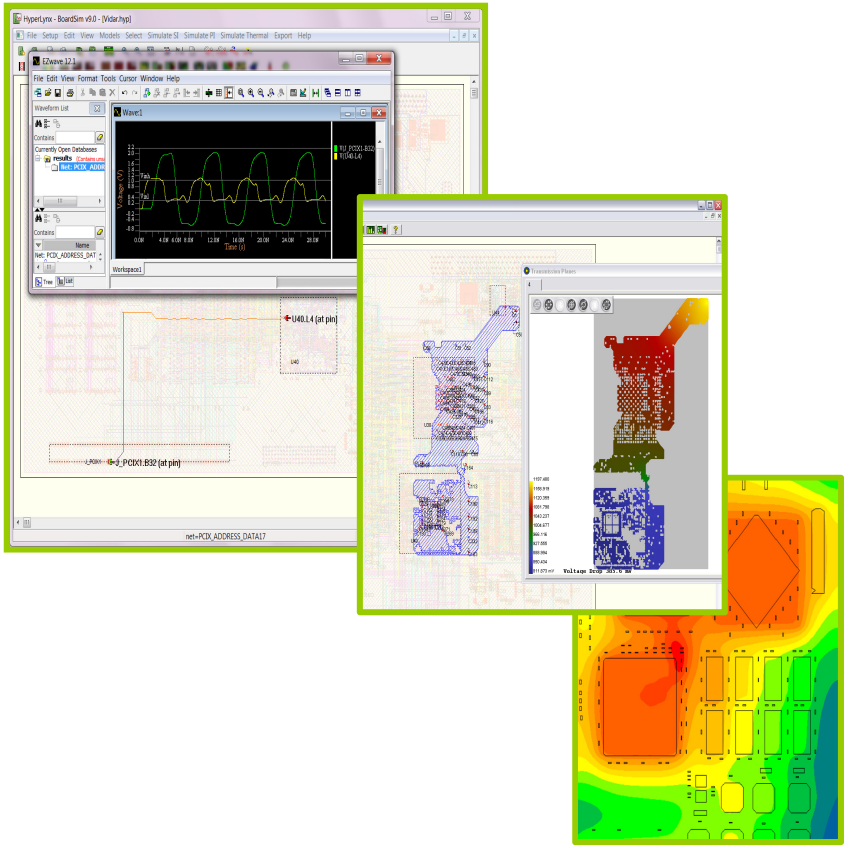


HYPERLYNX 9.1

Consolidated export from Xpedition

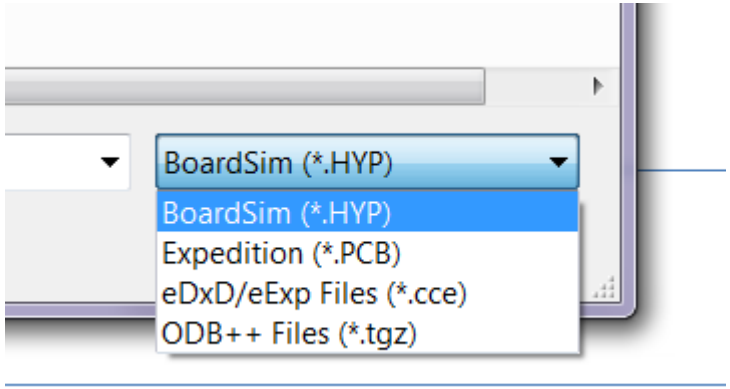
- HyperLynx SI and HyperLynx PI and HyperLynx Thermal all use the same exported file
  - Has info needed for all types of analysis
  - .CCE

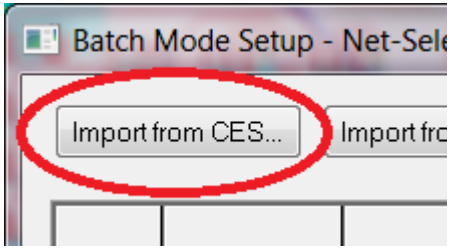




Improved Integration

- .CCE Import
  - —Both 64-bit and 32-bit
- ODB++ Import
  - —Both 64-bit and 32-bit
- Read in SI Constraints
  - —from .CCE file
  - —into Generic Batch Mode
- Read in DC Drop constraints
  - —from .CCE





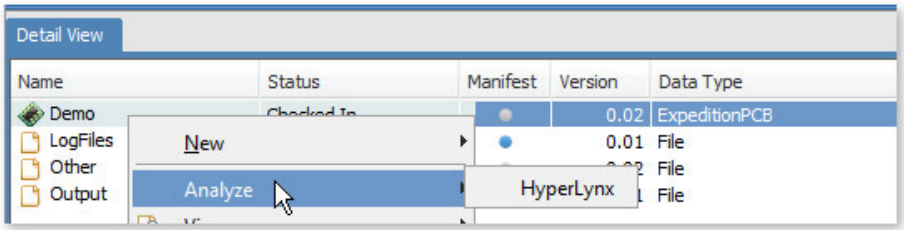
Enhanced EDM integration

- HyperLynx LineSim Support
  - LineSim is now fully supported in EDM and all the required HyperLynx files (*.ffs + *.pjh) are saved together with the DxDesigner project file at check-in

- HyperLynx BoardSim Enhancements
  - Automatic design synchronization between Xpedition, EDM, and HyperLynx
  - Metadata enhancements
  - Support for concurrent analysis

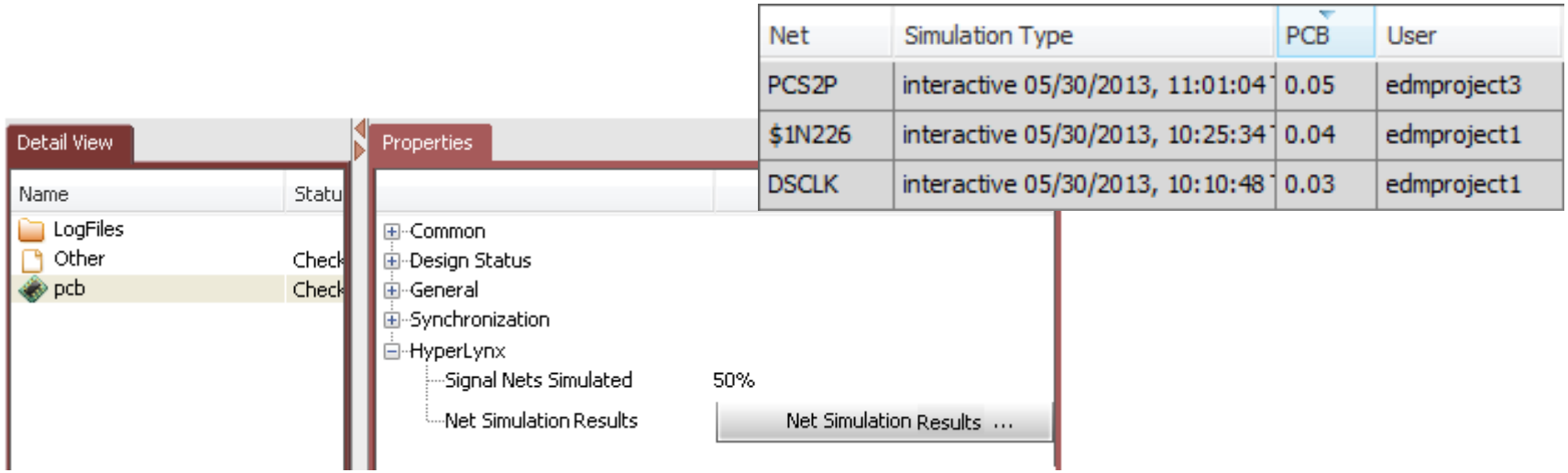
EDM synchronization

- Starting with VX release, Xpedition and CES automatically generate design and constraints data (.CCE and .CSE files) on each checkin of the design
- HyperLynx uses this data for analysis, thus providing automatic synchronization with a specific version of an Xpedition design
  - No need to manually export the data for high-speed analysis - it's always available at hand



Design state information

- Once analysis is run, the result is shown as meta-data of the PCB design. The following information was added:
  - PCB design version used to perform analysis
  - Name of the user



EDM concurrent analysis

- Multiple users will be able to analyze a design simultaneously
- Analysis can be done on different computers – local settings, including IBIS models, will be preserved for each user and automatically restored on the same or a different machine
  - Settings can be reused when analysis is done again with a newer version of the design
- Analysis results from multiple users will be automatically combined and displayed as metadata

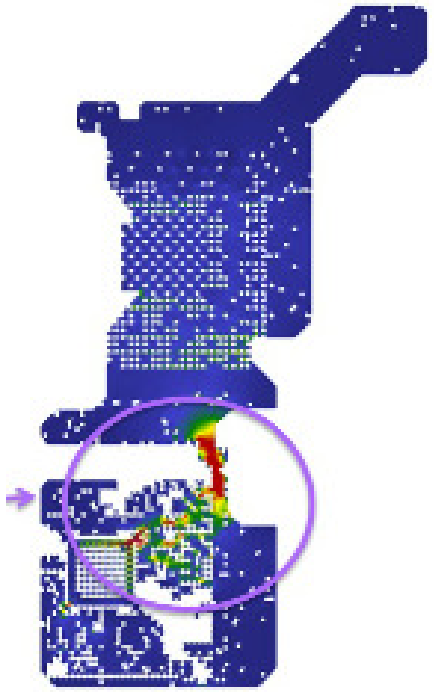
Also New in VX (HyperLynx 9.1)

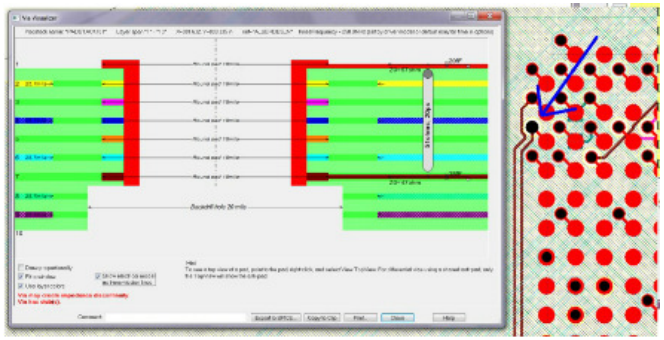
- New Toolbar icons
  - With enhanced tool tips
- Language localization (Chinese)
- Show full path in recent files and title bar
  - Idea #D2862
- New editing modes in the stackup editor
  - Keep CES and Expedition stackups in sync
  - Option to turn off Z0 calculation to improve performance
- QPL editor in LineSim
- Touchstone Viewer
  - now supports Touchstone 2.0
  - TDR plot smoothing

HYPERLYNX 9.X TEASER

HyperLynx 9.2 Main Features

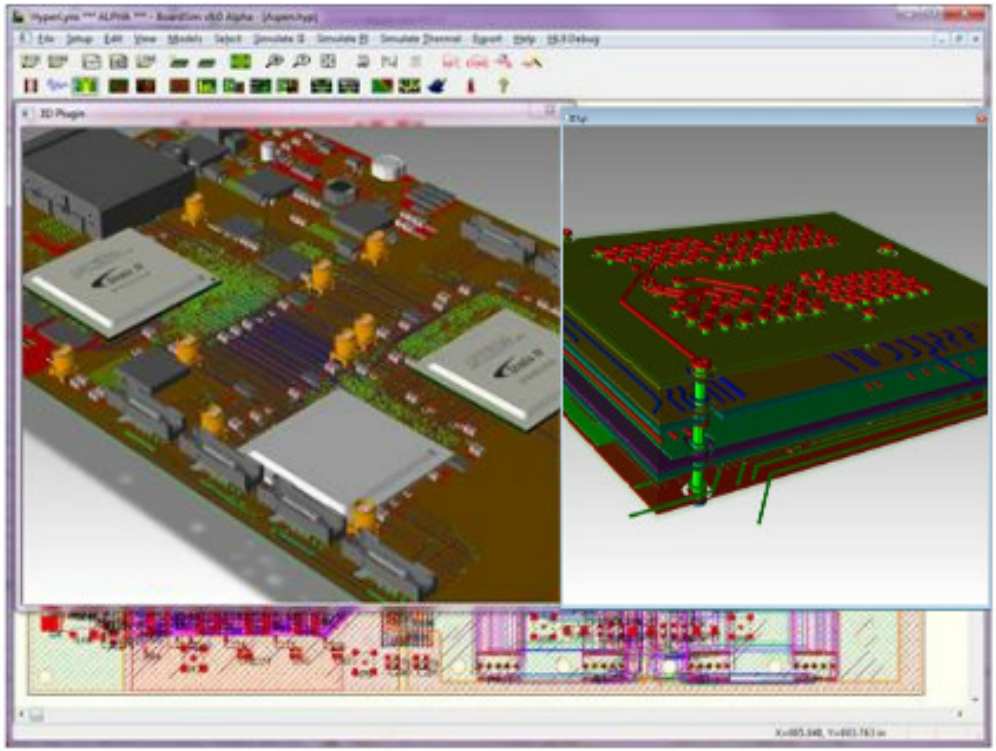
- Multiple Net Selection
- (LP)DDR4 Support in DDRx Wizard
- Back drill support
- SERDES Improvements
- Advanced S-parameter Extraction
- IBIS Model PI effects
- PI Pin grouping
- DC Drop performance improvement (x20)





Hyperlynx 9.2 3D Viewing

- Integrated 3D board and region viewing
- High performance display of entire PCBs, including realistic lighting and shading, etc..
- 3D view of selected areas/objects for detailed studies



www.mentor.com