

# Expedition Enterprise Product Update

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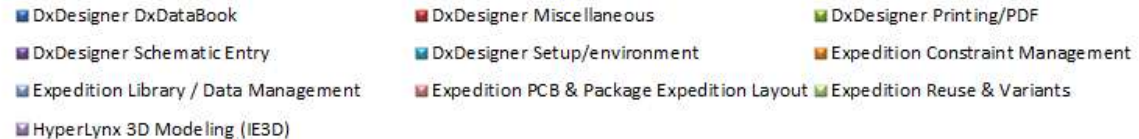


# Presentation Overview

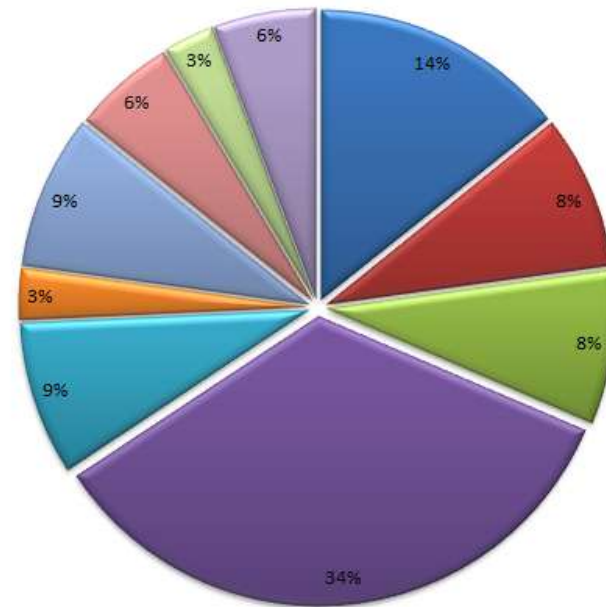
- EE7.9.3 release update
- Planned releases (EE7.9.4/5)
  - Mentor Ideas
  - DxDesigner
  - DxSystems Designer
  - Expedition, CES
  - DMS
  - FPGA Design



# 35 Customer Ideas Delivered in EE7.9.3



- At least 8 ideas targeted for 7.9.4
- At least 15 strategic ideas currently marked as Planned

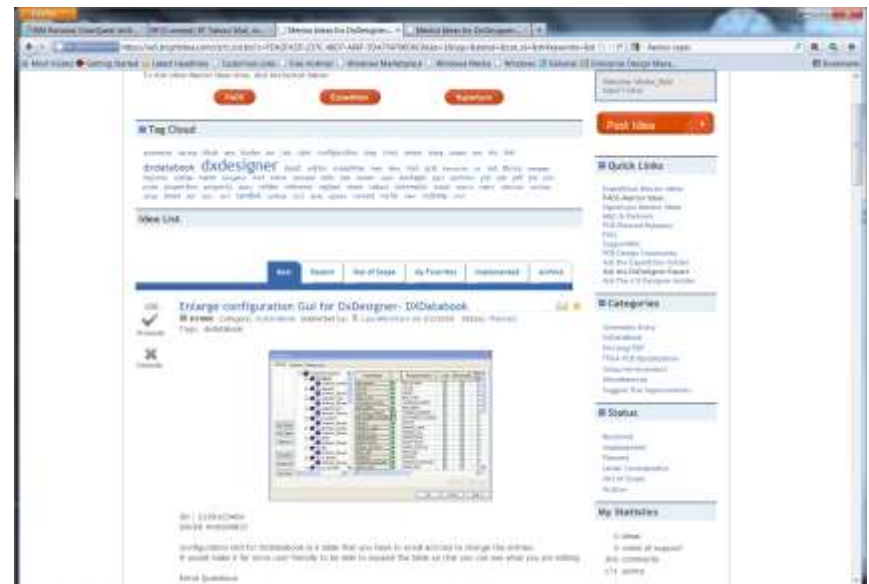


# DxDesigner, DxDataBook

## Addressing the Top Ideas

EE 7.9.3

- Top Ideas on DxDesigner web site
  - D1868 – Enlarge the configuration GUI for DxDataBook
  - D1749 – Want pin numbers displayed when placing parts from DxDataBook
  - D1647 – Global filter for cross-probing

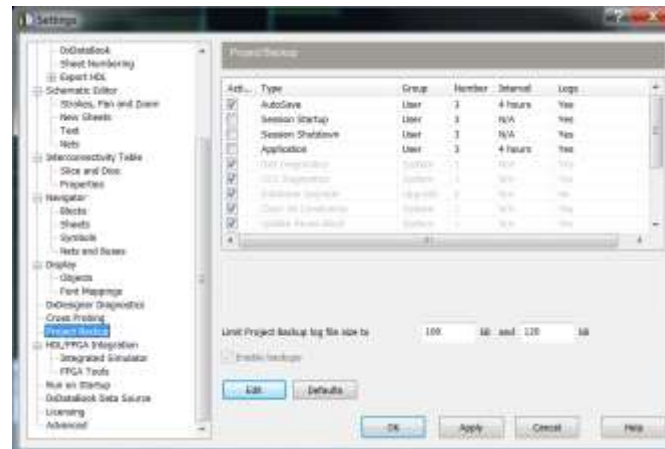
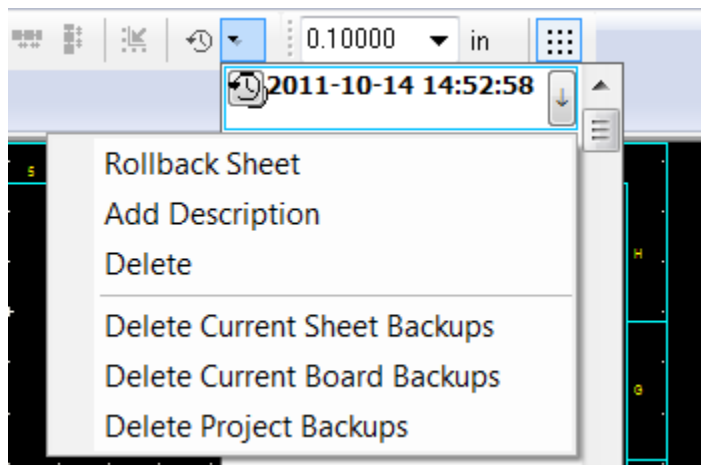
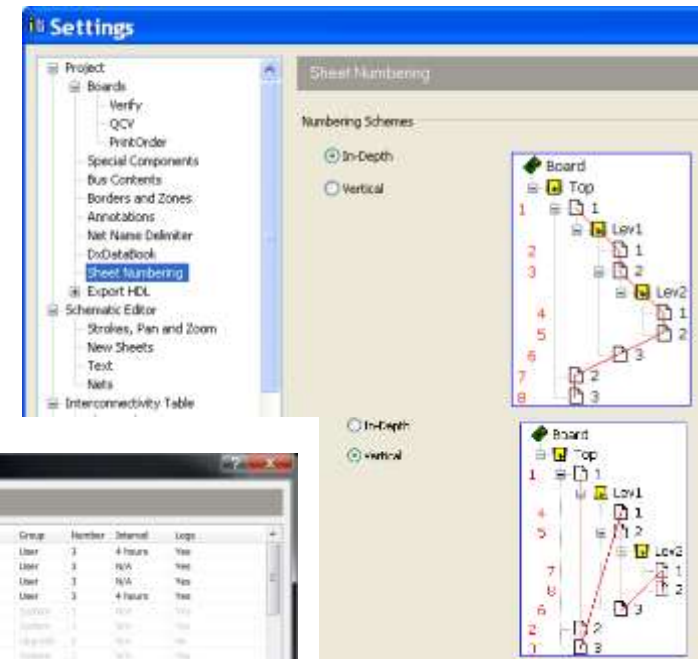


# DxDesigner

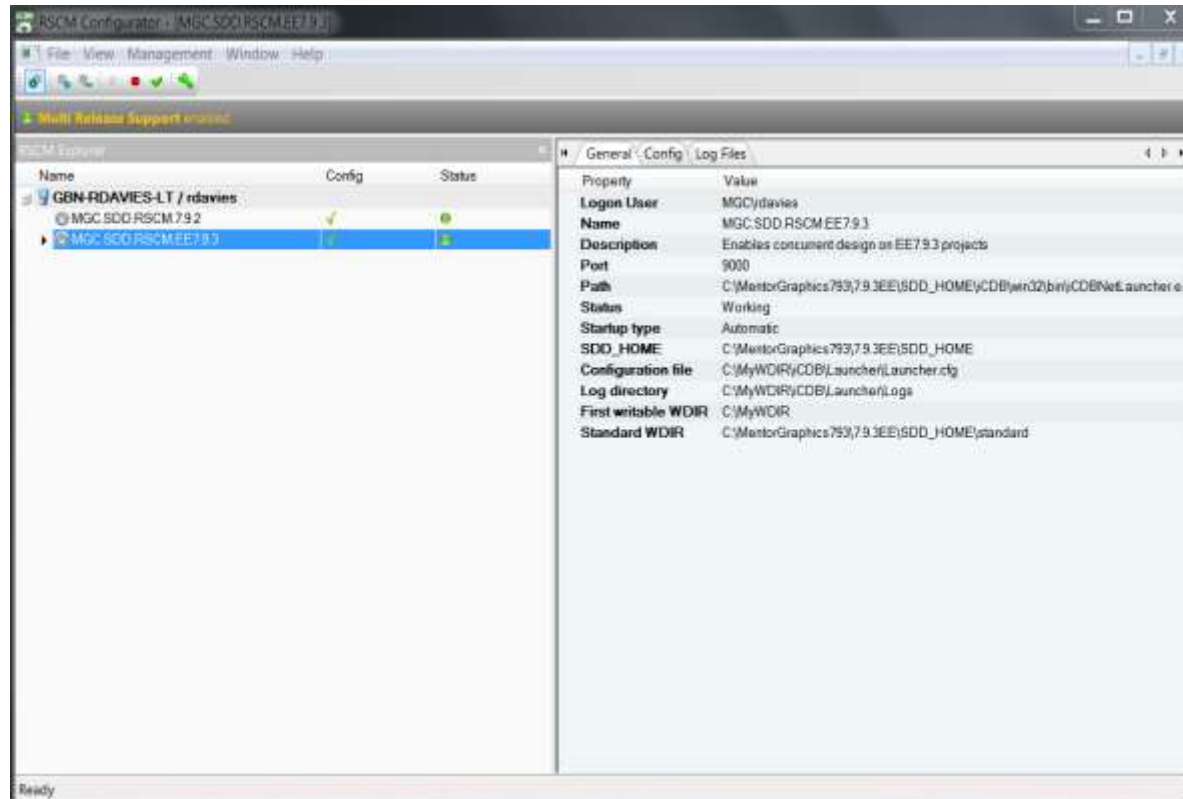
## Schematic Editor Enhancements

EE 7.9.3

- Sheet numbering / print order
- Autobackup
- Sheet backup / rollback



- RSCM/iCDB Server improvements
  - RSCM Configurator to handle multiple versions of Server
    - Setup OS for user log on
    - Setup pathmaps.cfg



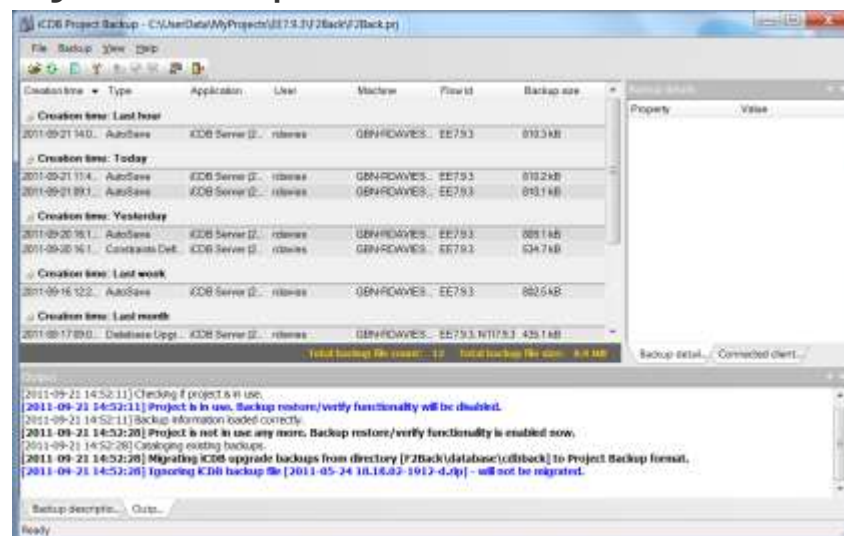


# Infrastructure

## iCDB Project Backup

EE 7.9.3

- Include Expedition PCB data in the backup
- Recognize DxDArchive in Project backup
  - Provide option to restore from Archive
- Provide REPAIR PROJECT and REPAIR BACKUP options
  - iCDB will attempt to repair the database
- Provide “Project Support Package” function
  - Gather necessary files in a zip archive
- Provide Cleanup option to be used in Project Backup
  - Remove unnecessary log/report files
- Provide functionality to run a Backup on demand



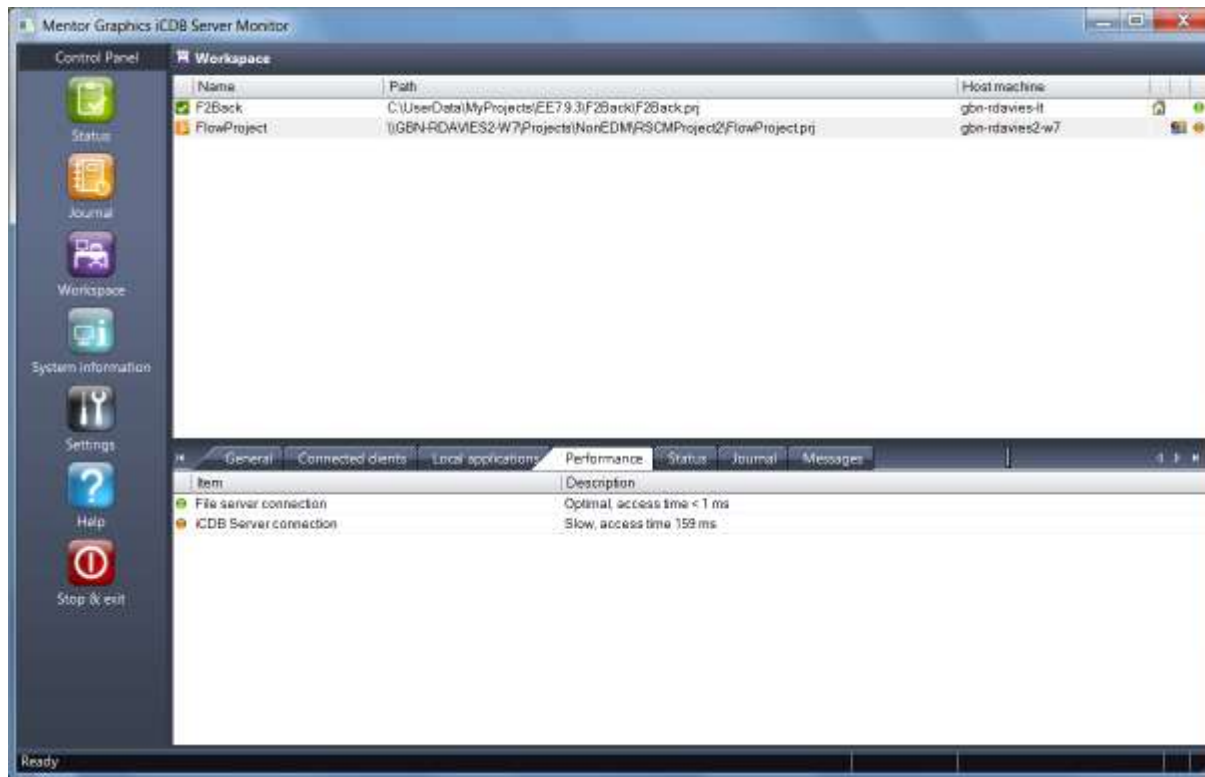
# Infrastructure

## iCDB Monitor

EE 7.9.3

### ■ New workspace view

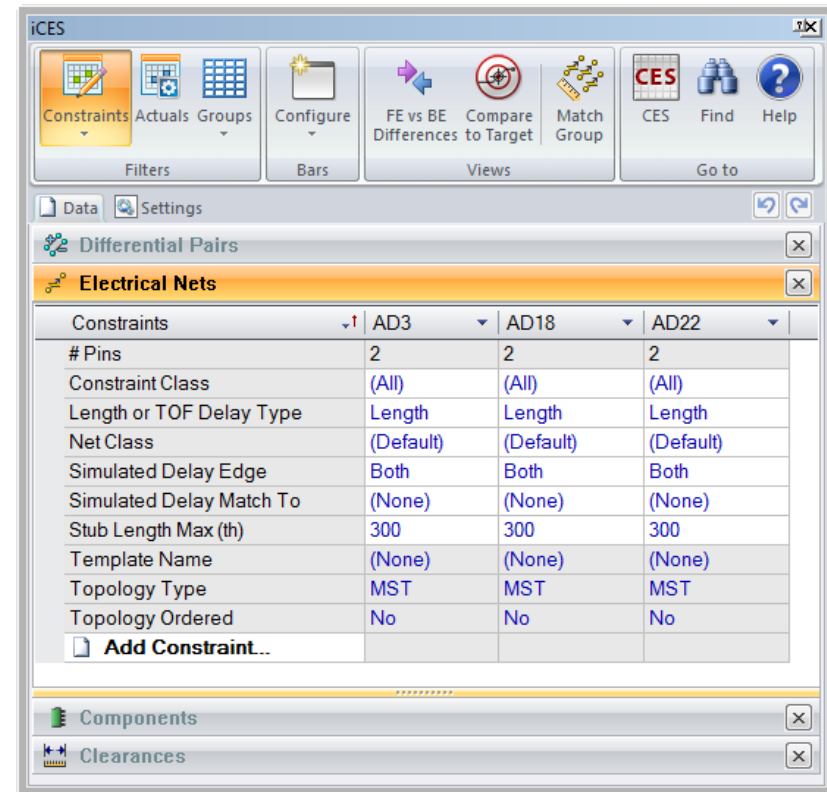
- Shows additional information about connected clients
- Includes performance of iCDB Server connection and file server connection



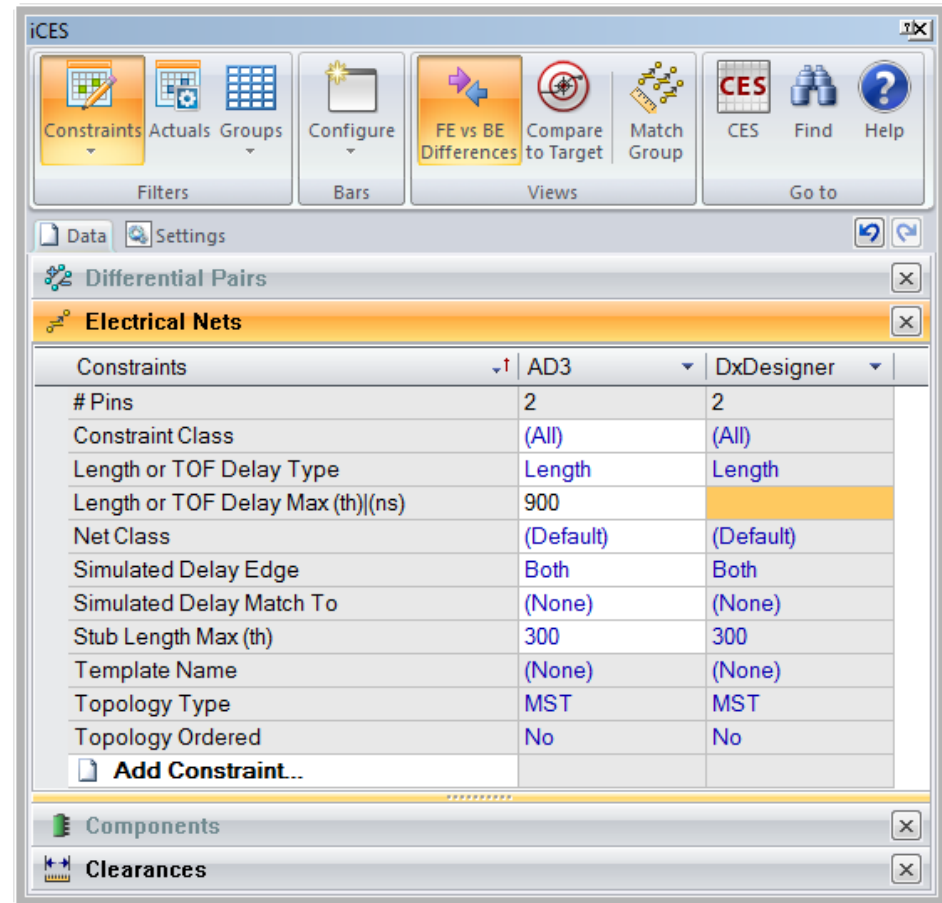


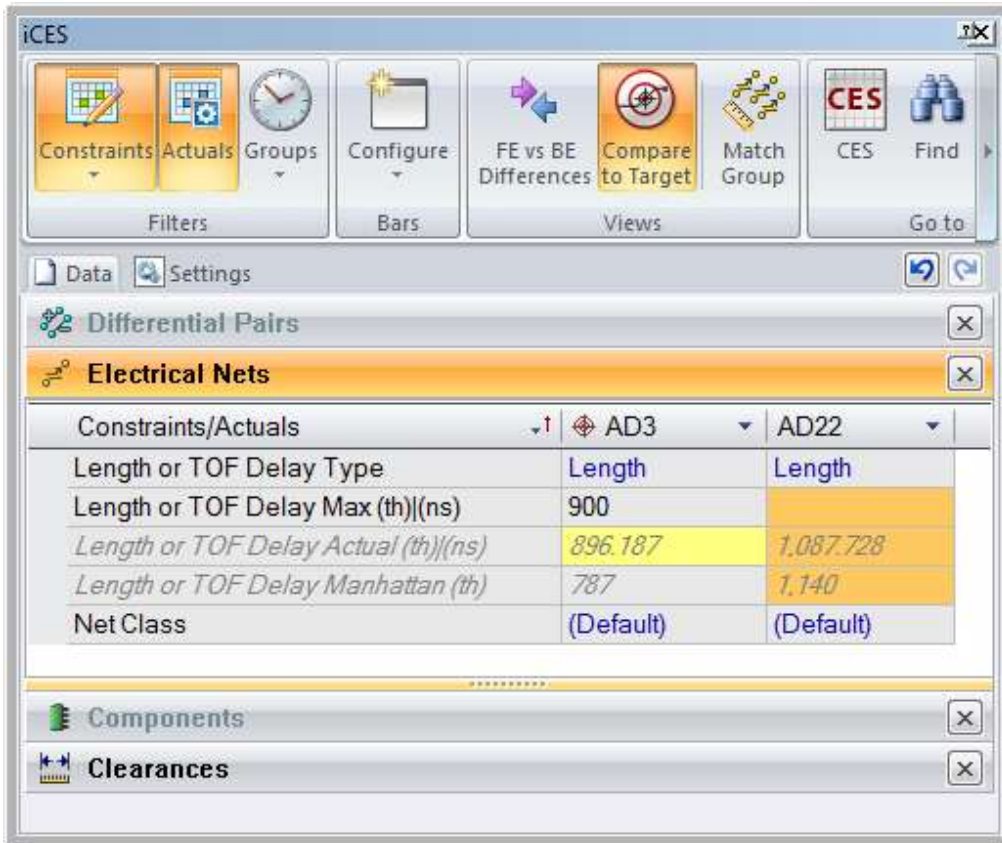
# Introducing iCES

- The next step in evolution of constraint management
- View or edit most commonly-used constraints within the host PCB editing tool
- Context-driven operation
  - Constraint data for the object(s) selected within the host
- Optimized to view relevant data
  - Can easily refine the view to further optimize
- Easy to learn / easy to use
- Add-in to a PCB design tool
  - Hosted by DxDesigner & Expedition in initial release



- Productivity booster for DxDesigner, CES & Expedition PCB
  - Intuitive to learn
  - Easy to use
  - Find & edit constraints faster than CES
- Shorten design cycle time
  - Real-time access to relevant constraint data
  - Unique features enabled thru add-in architecture

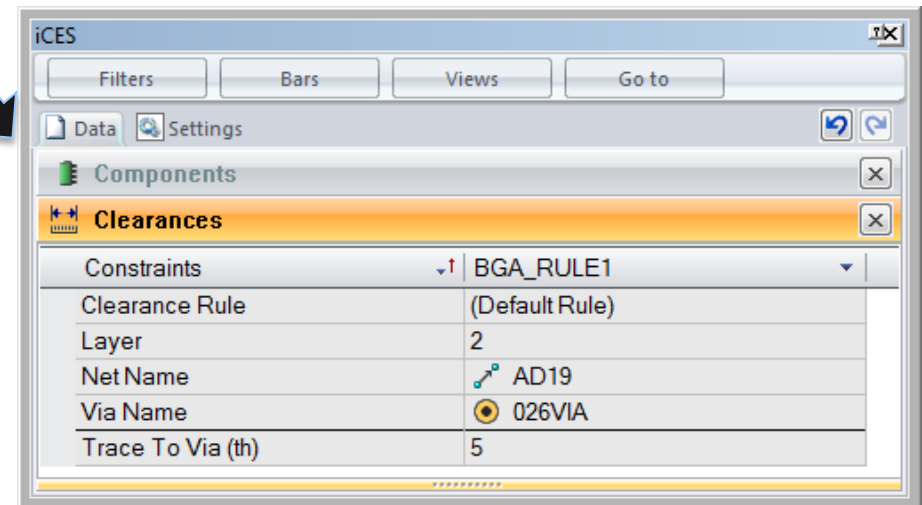
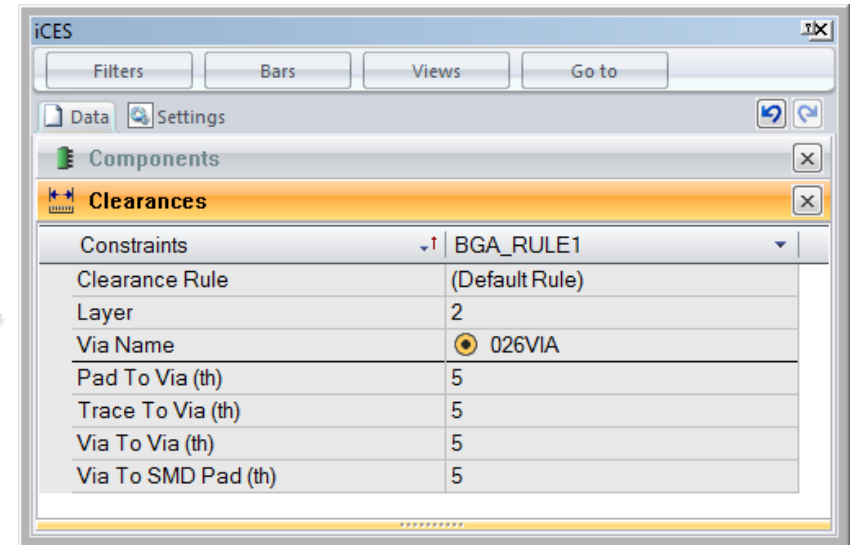




- Modern, dock-able, configurable GUI
- Simple & powerful filtering
- Basic constraint editing
  - View
  - Edit
  - Add
  - Viewing Actuals
- Advanced constraint editing features
  - Front-end vs. Back-End
  - Compare to Target
  - Match Groups
- Concurrency support
  - XtremePCB support

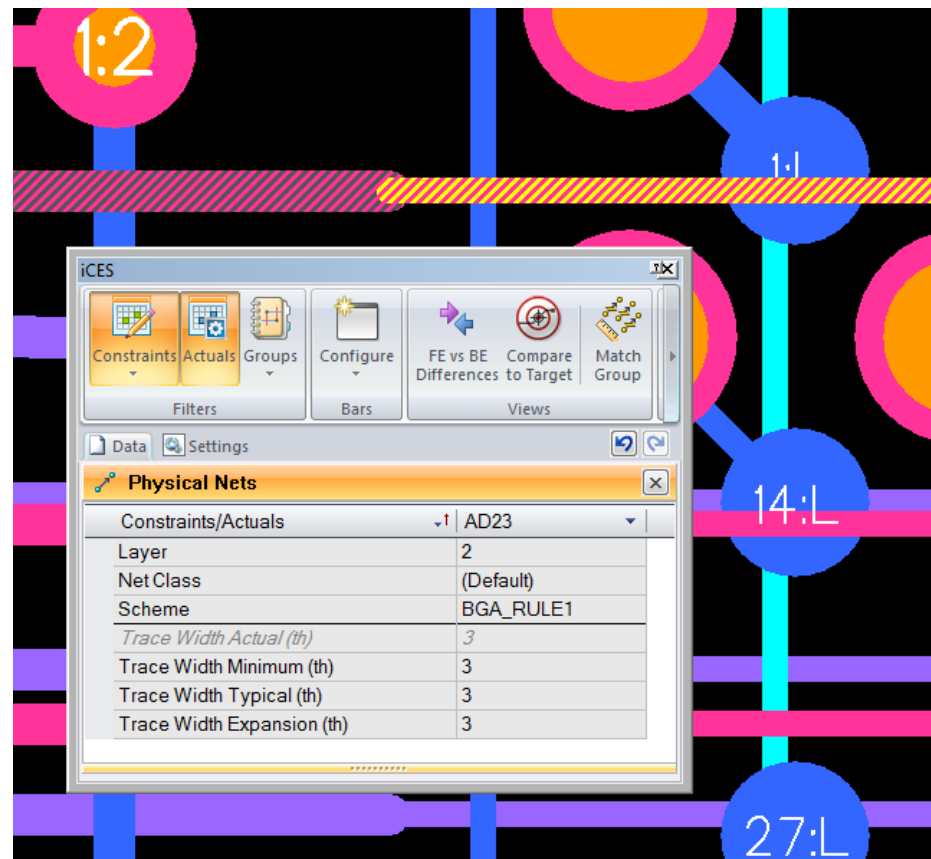
# Clearances Support

- New bar to display clearances
- View clearance rules for single object
  - To other objects
- View clearance rule between two objects
- View actual distance
- Supports most common objects
  - Traces, Vias, Pads



# Widths Support

- Ability to view trace widths
  - On physical nets only
- Includes new group “Trace Widths” and displays
  - Layer
  - Net Class
  - Scheme
  - Minimum
  - Typical
  - Expansion (if defined in CES)
- Actuals supported
- Feature designed to be used on nets/segments on a single layer



## 7.9.3 Overview

### DMS Desktop GUI

- DMS welcome page
- DMS perspectives
- Improved search window
- Improved information (object details) window
- Intuitive search references

### Administration

- Auto installation of Tomcat
- Creation of catalogs/objects from catalog objects

### DMS Designer

- Login from DxDataBook
- Library researcher enhancements
- Part request copy

### Library process

- Library flow manager enhancement
- Improved PDF generation
- Support long pin numbers

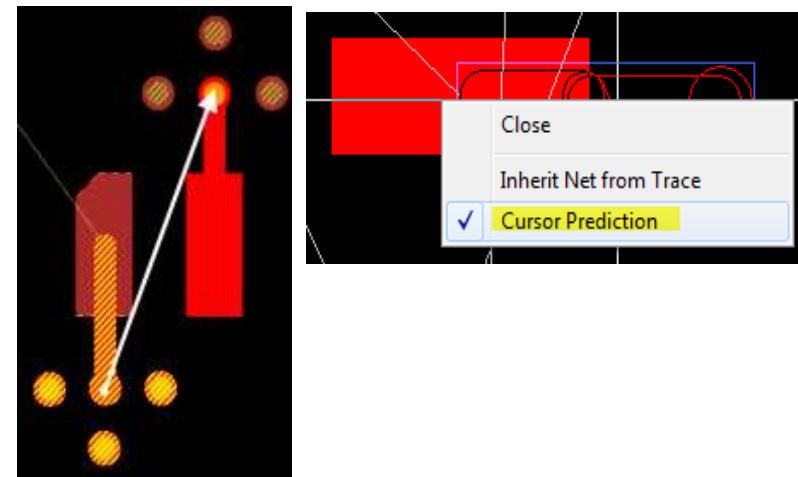


# Expedition PCB

## Copy Trace

EE 7.9.3

- Copy Trace with Cursor Prediction
  - New RMB menu item to turn Cursor Prediction off
  - No prediction if source & target outside of graphical view
- Improved support for mix of (un)connected objects
- Improved support for “dx=X,Y” keyin

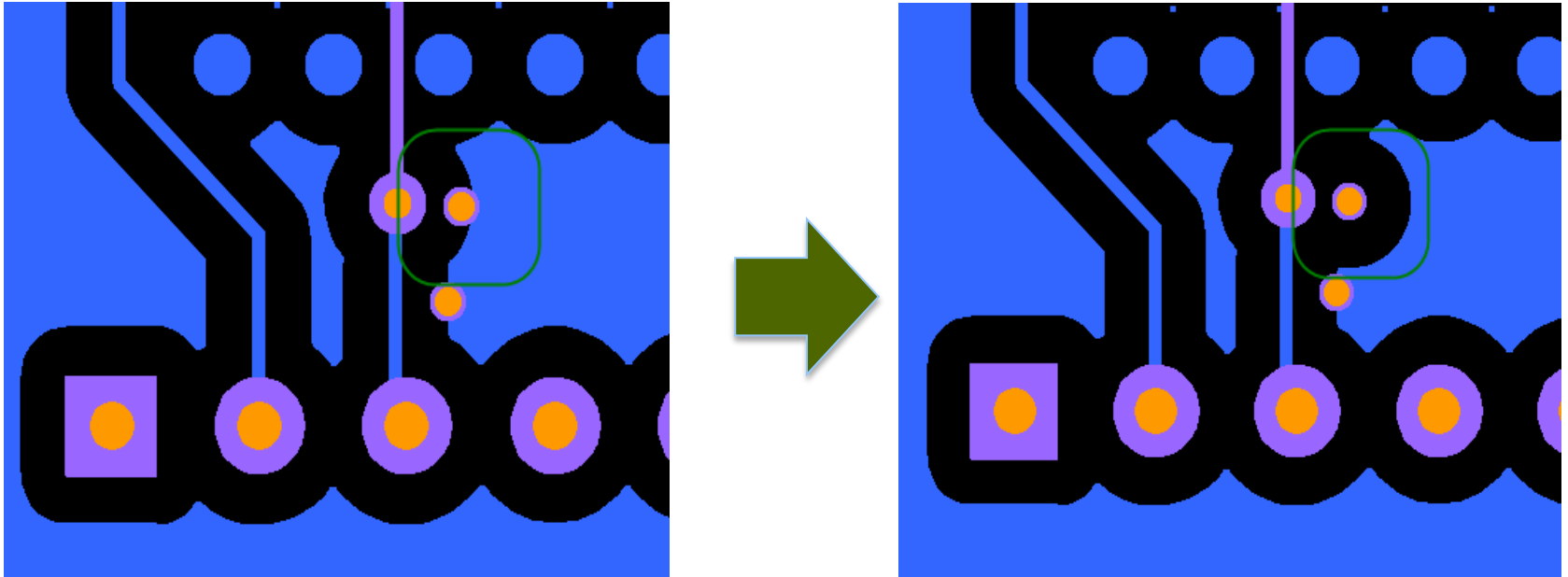


# Expedition PCB

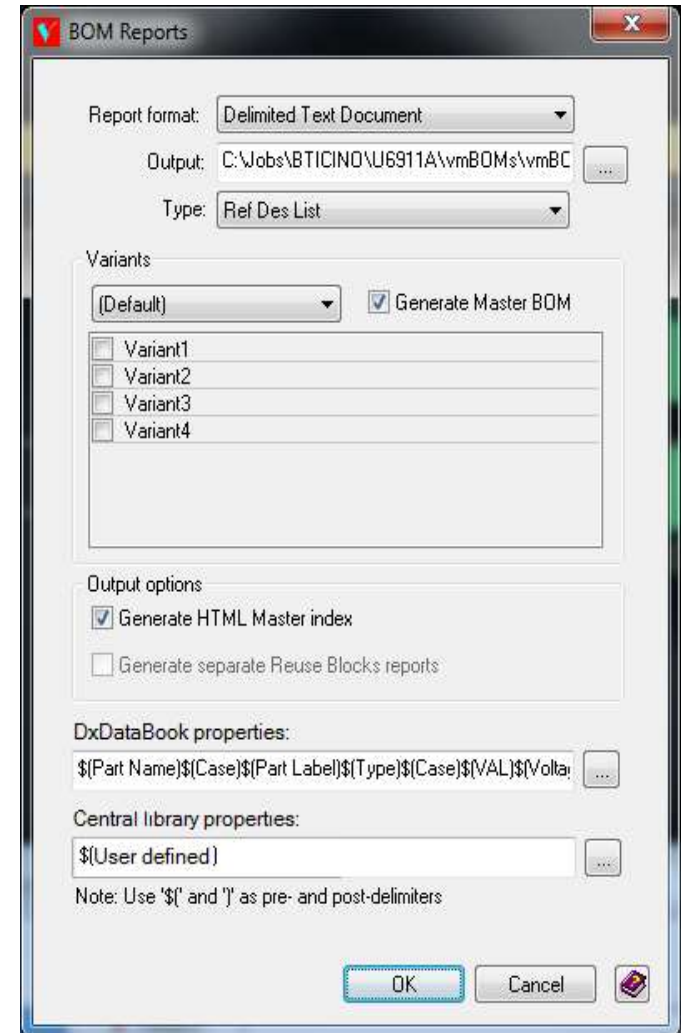
## Dynamic Planes

EE 7.9.3

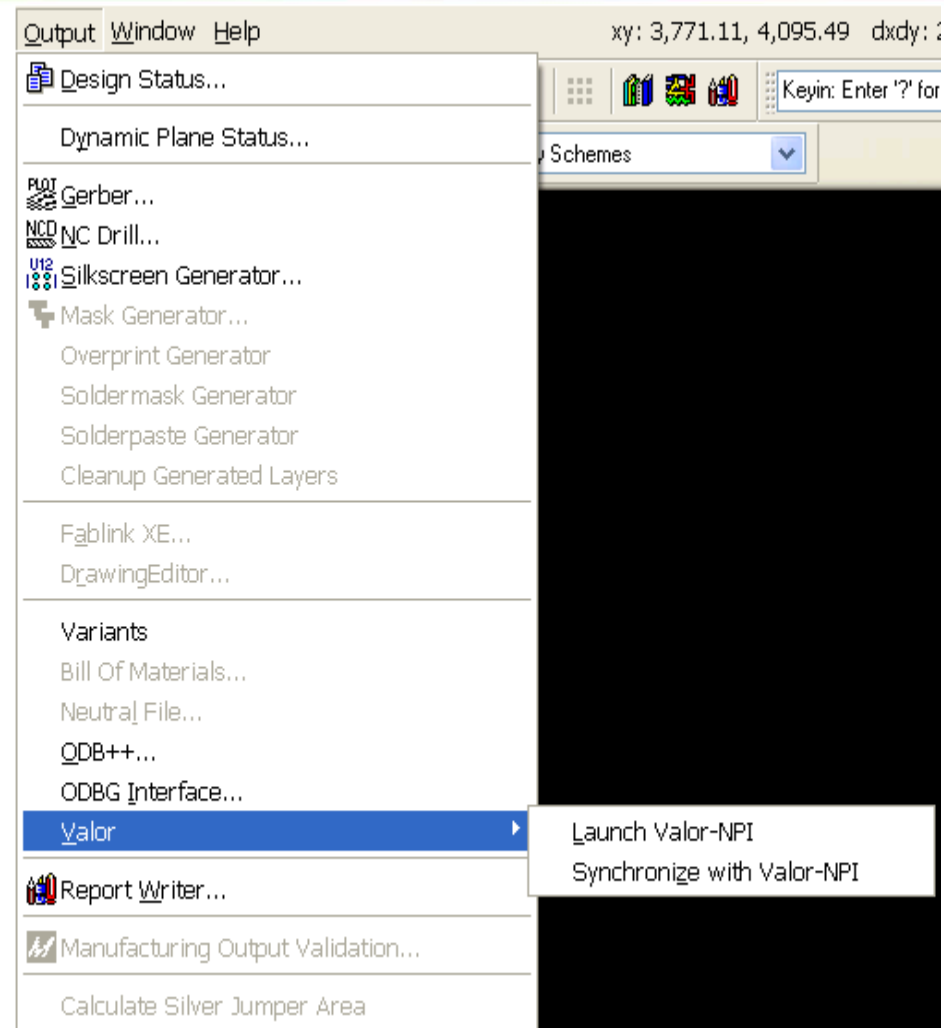
- Buried connections
  - No connect when pad origin is outside of user-input plane shape
  - Now applies to plane sub-shapes
- Improved DFM when a connected pad is on the edge of a clearance area.



- In 7.9.2, only DxDataBook properties were available for output
- In 7.9.3, additional Central Library properties, including user-defined properties, are available
  - Available within Variant Manager BOM output
  - Same list selection as for DxDataBook properties



- DFF, DFA and DFT analysis within the Expedition flow
- Cross probe between Valor NPI and Expedition PCB
- Review analysis results in Hazards
- Minimize iterations with manufacturing
  - Valor NPI users average 57% *fewer* revision spins than non-Valor users
- Fewer major production issues
- Time savings in release schedule
- Optimize hand-off to manufacturing with ODB++

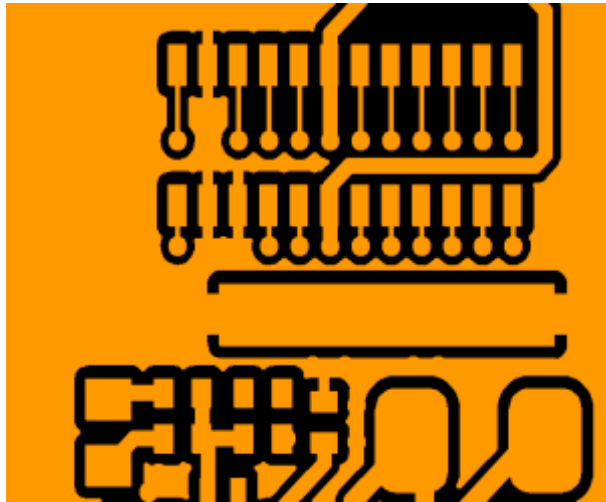


# Expedition PCB

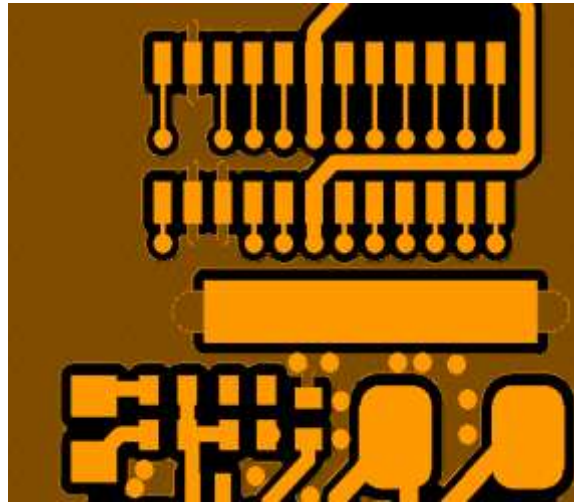
## Plane Metal Display

EE 7.9.3

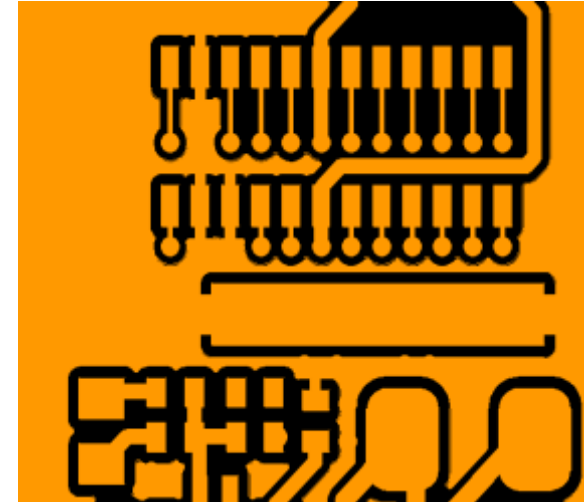
### ■ Improved static metal display



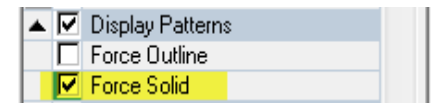
State: Dynamic



State: Static with Pattern



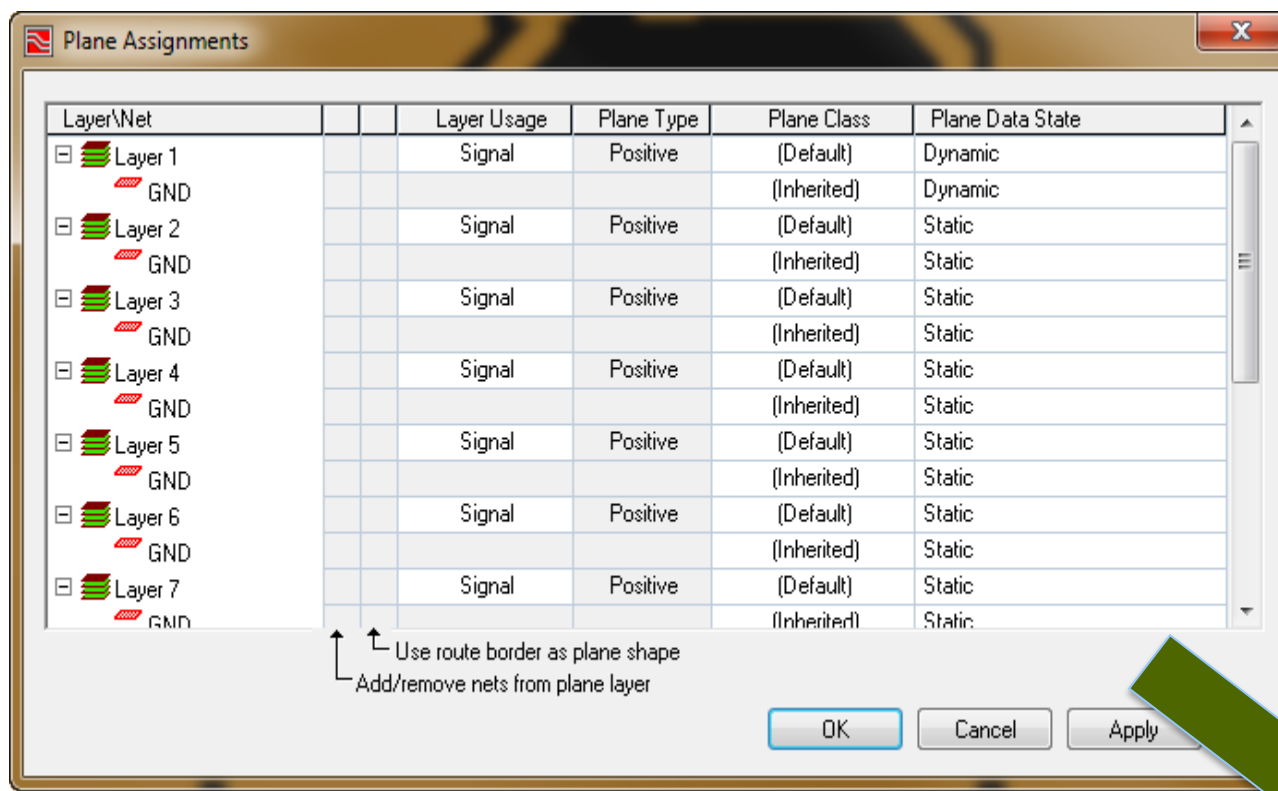
State: Static with Forced Solid



- Static Patterns indicate metal is not dynamic
- Expedition PCB/Viewer/Browser can now display static metal as Solid

## Plane Assignments GUI

- Plane Assignments GUI is now stretchable
  - Display more layers/nets in a larger area



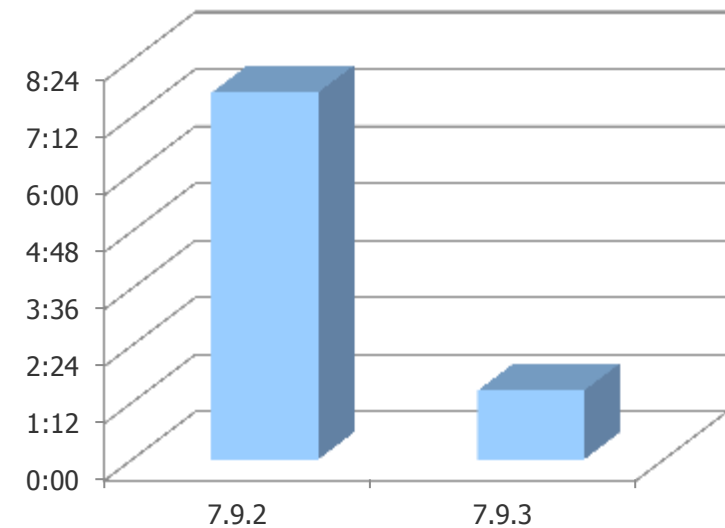


# Expedition PCB

## Improved Performance

EE 7.9.3

- Improved performance of Expedition and Xtreme PCB startup
  - IC Package designs with huge numbers of component pins
  - 7.9.2: 7:43 mins vs 7.9.3: 1:27 mins
  - Up to 80% improvement
- Improved performance also seen with:
  - Forward Annotation
  - Xtreme
  - Setup Parameters
  - Features that require a design re-load.



# Product Plans

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## ■ DxDesigner

- Usability mission
  - Improved out-of-the-box experience
  - Usability improvements
- Documentation (PDF)
- Compound symbols

## ■ DxSystems Designer

## ■ Expedition, CES

## ■ DMS

## ■ FPGA Design

# DxDesigner Usability Mission

## ■ Customer value

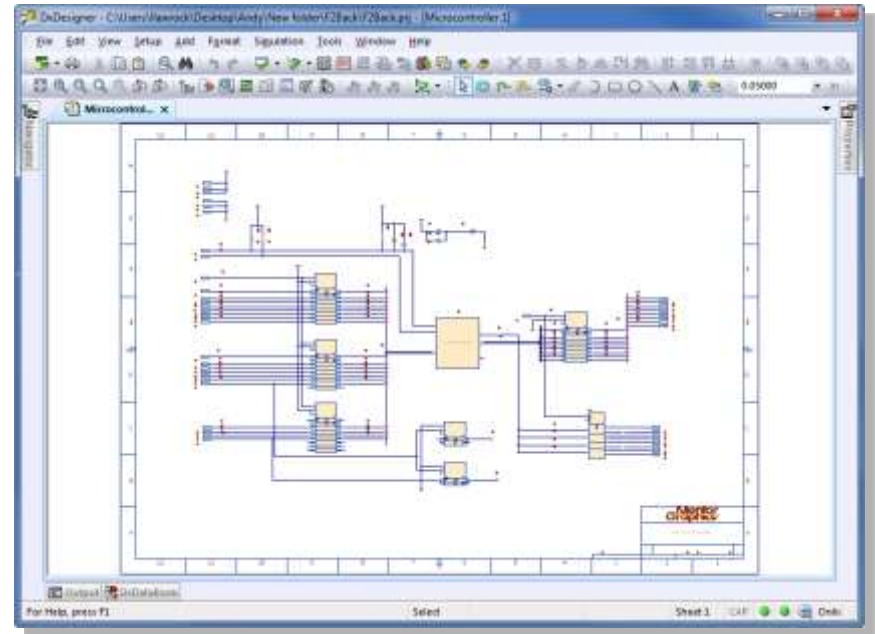
- Enable engineers to focus on product development and not on tool usage
- Address needs of casual users
- Reduce learning curve
  - Minimize training effort and cost
- Increase productivity
- Lower the bar for tool unification across the organisation
  - Easier administration
  - Enables reuse
  - Benefits of better flow integration
  - More synergy between departments





### ■ DxDesigner usability improvement project throughout 7.9.4, 7.9.5 and beyond

- Graphics improvements
- Editor enhancements
- Usability enhancements
- Ultra-modern look and feel
  - Common across all platforms
- Out of the box (OOTB) configuration enhancements
  - Also includes start-up screen
- Documentation enhancements

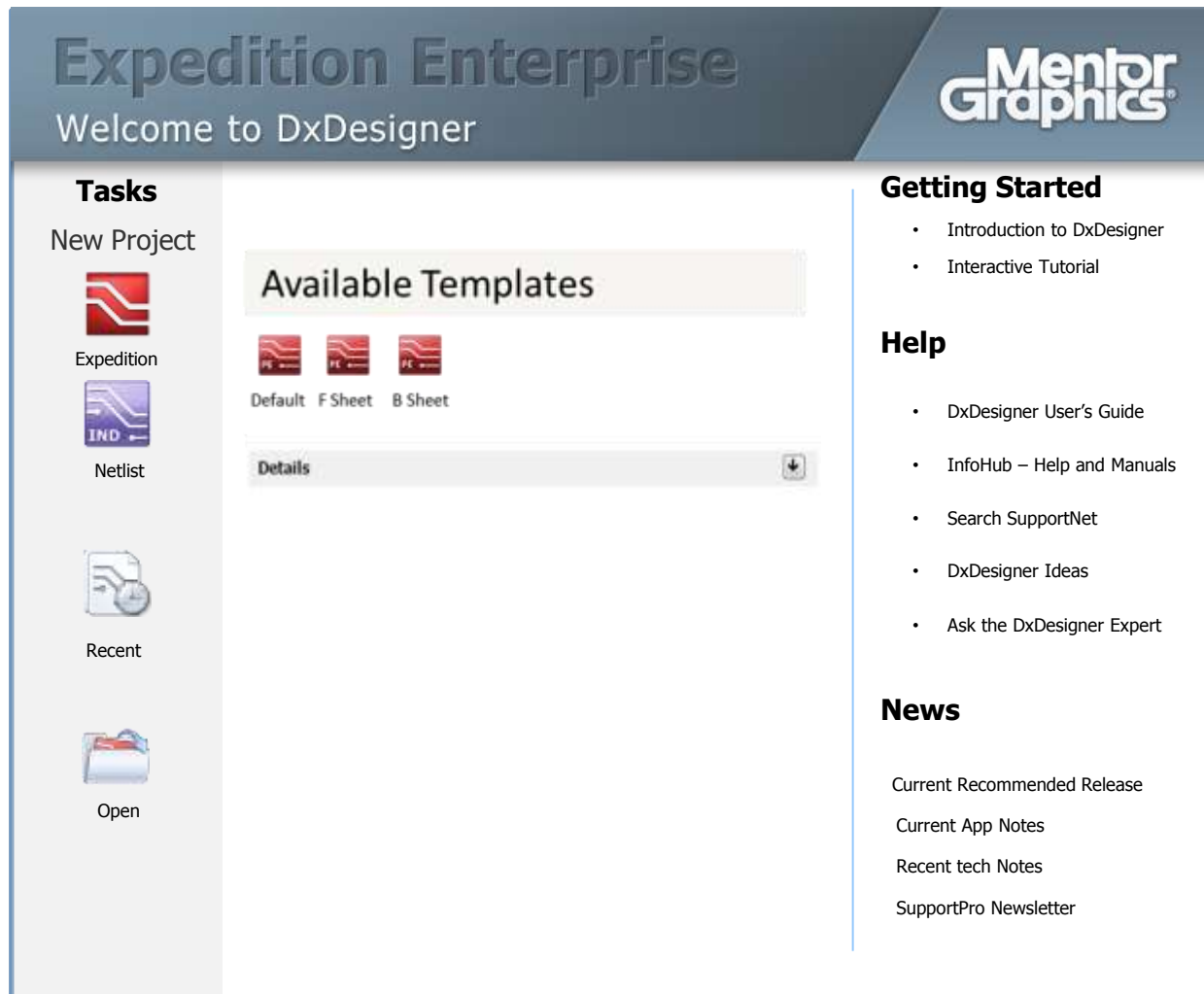


# DxDesigner

## Start-up Screen

EE 7.9.4

- Quick access to tasks and useful information





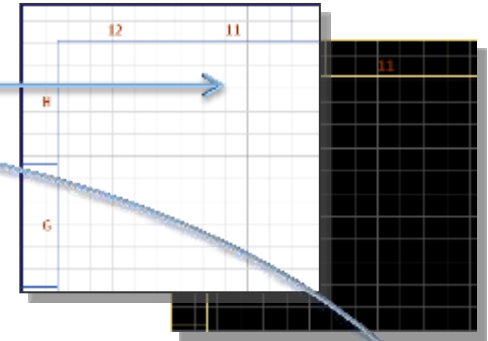
# DxDesigner

## Usability Improvements

EE 7.9.4

### ■ Graphics improvements

- New grid
- Pan & zoom
  - Super view window
  - Improved panning -smooth move
- Layered graphics (foreground/background)

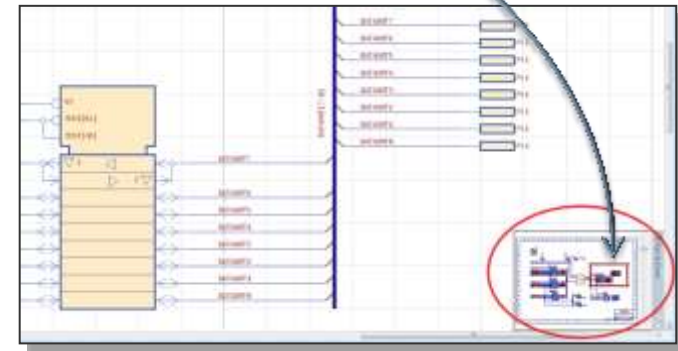


### ■ Improved text management

- In-line & multi-line editing
- System fonts exposure

### ■ Dynamic graphic violation highlight and fix

- Batch mode (dynamic in 7.9.5)
- Highlights and fixes text overlapping with:
  - Nets, symbol graphics, properties and other text etc.



### ■ Improved routing (wiring model)

- Continuation of efforts from 7.9.3 throughout 7.9.4, 7.9.5 and beyond
- Rubber banding nets/symbols avoiding violations and overlaps

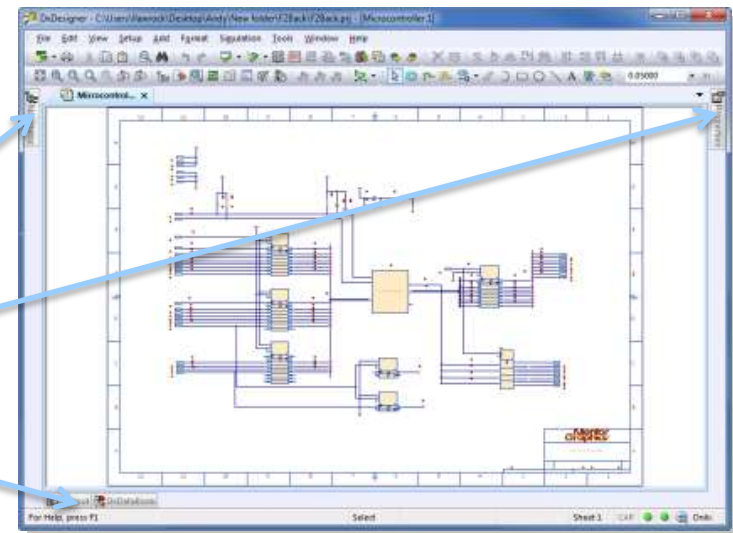
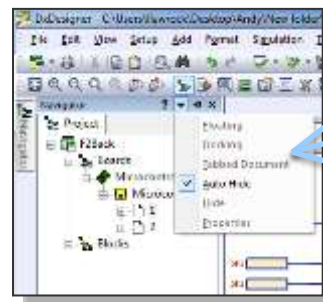
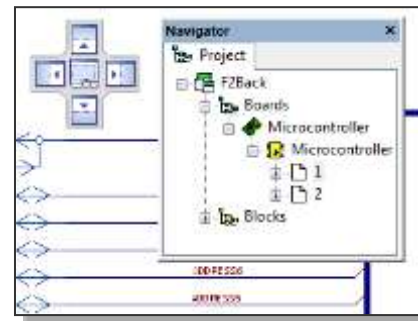




# DxDesigner Usability Improvements

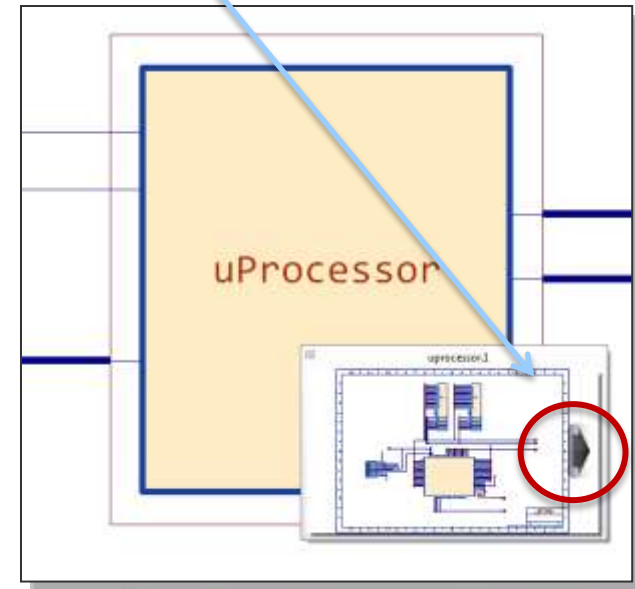
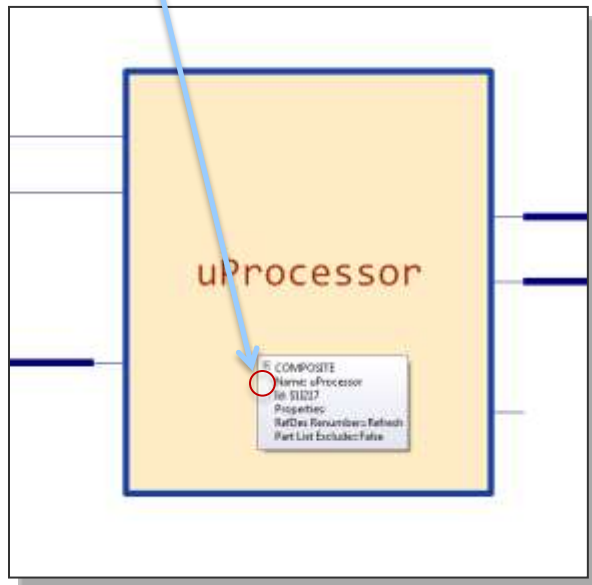
EE 7.9.4

- Ultra-modern Windows-like layout on all platforms
  - 24-bit color depth toolbars
  - Window layout
    - Docking/undocking
  - Sliding windows
    - Auto hide



## Tool Tip Hierarchical Preview & Navigation

- Thumbnail view of the underlying hierarchical block for easy navigation to the schematic contents
  - Select "+" in tool-tip to view thumbnail
  - Double click thumbnail to open schematic
    - Click the arrow to navigate to other sheets

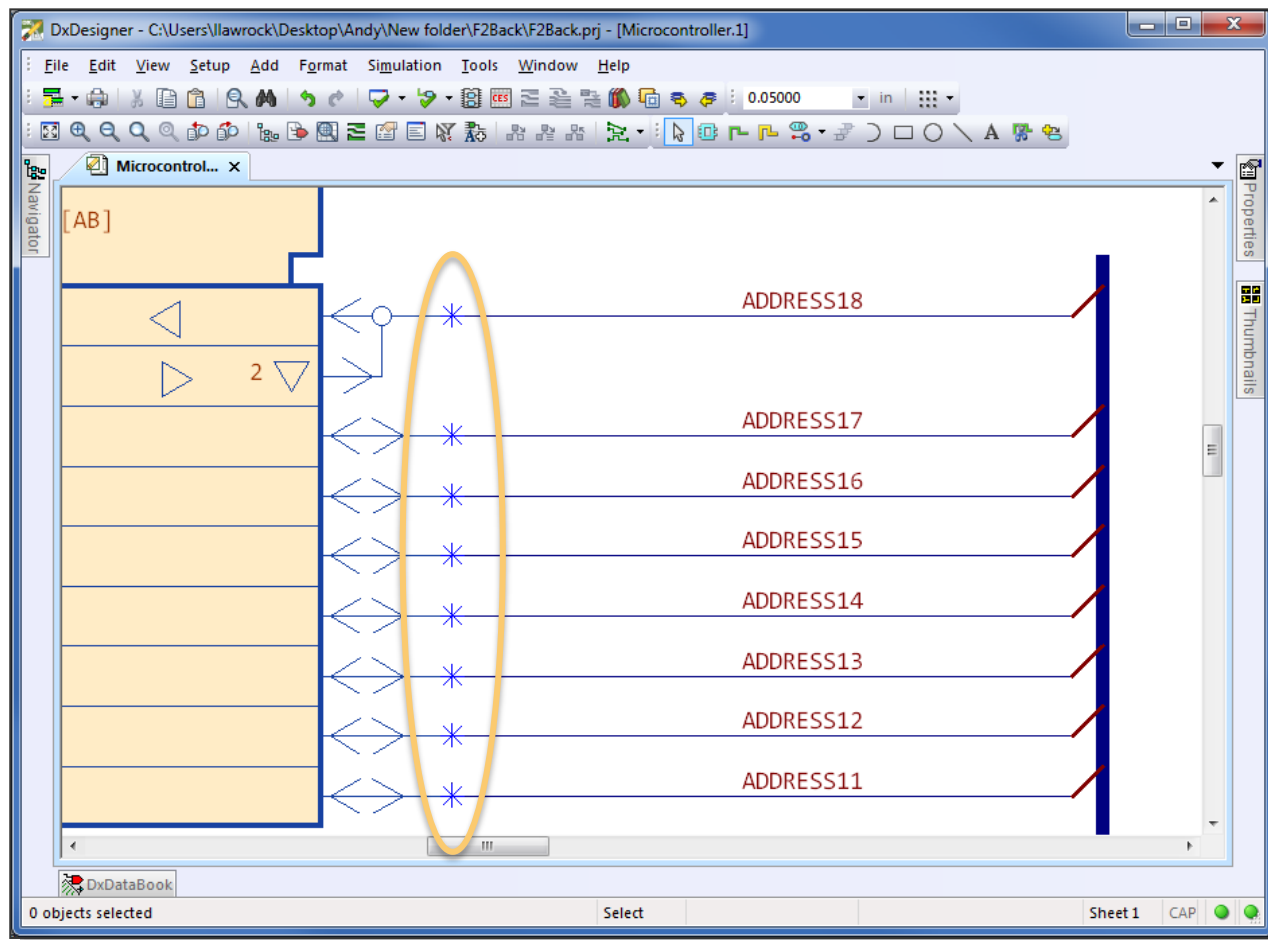


# DxDesigner

## Connectivity Advisor

EE 7.9.4

- Visual indication as user closes in on complex net/bus connections





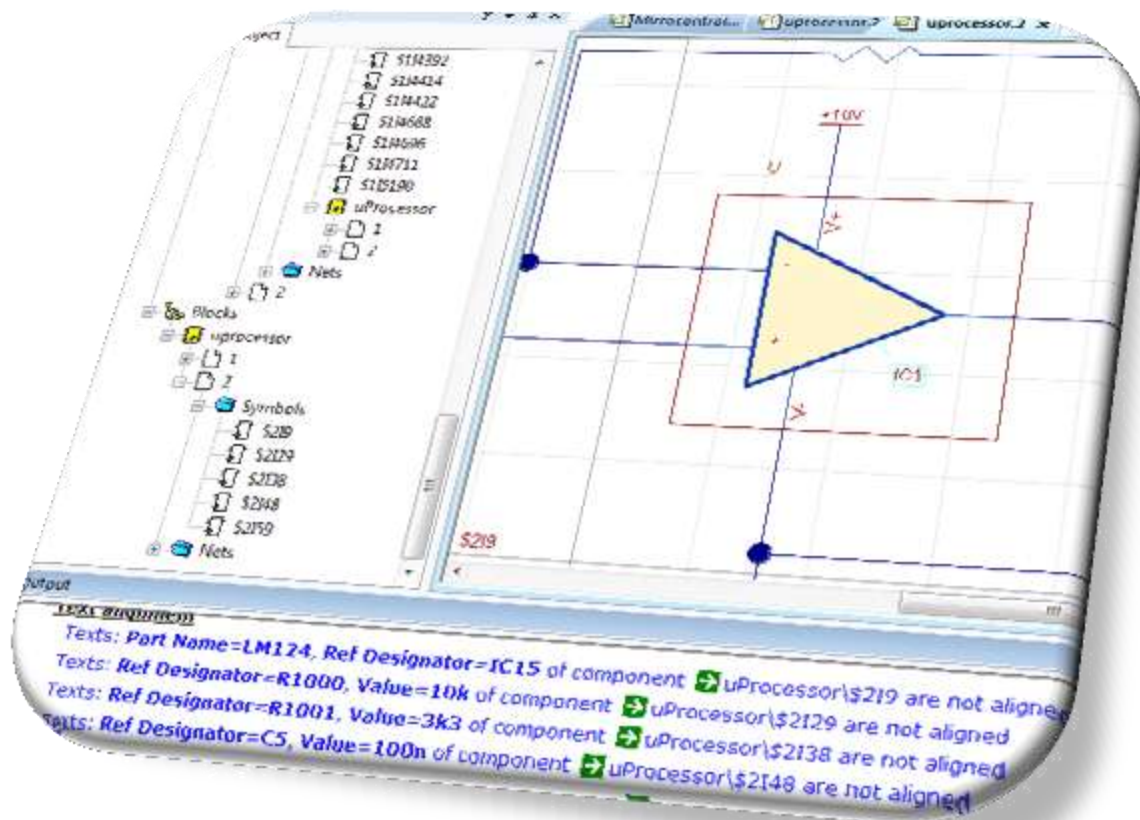
# DxDesigner

## Graphics Rule Checker

EE 7.9.4

### ■ Included batch checks:

- Off grid report
  - Off grid nets
  - Off grid pins
- Net overlap
  - Overlapping objects report
  - Object overlap
- Text report
  - Text alignment
  - Text owner



# **DxDesigner**

## **Usability Improvements**

EE 7.9.5

- Improved graphics/layout
  - Grab handles
  - Graphics scaling
  - Symbol placement via Visio-like categorized panels (DxDataBook)
  
- Maintainability
  - Integrated symbol editor
  - Compound symbol definition

# Product Plans

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- DxDesigner
- DxSystems Designer
- Expedition, CES
  - Expedition / Xtreme 7.9.4 focus
  - CES
  - NPI
- DMS
- FPGA Design

# Comprehensive Approaches to Systems Design

EE 7.9.5

## Single-board Projects

Mentor Solution:  
DxDesigner

- Single-PCB centric
- Engineering, logic, schematic at the board-level



## Multi-board Systems

Mentor Solution:  
DxSystems Designer

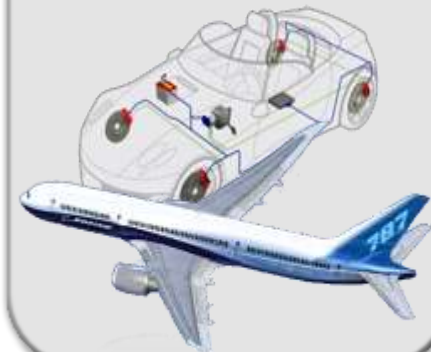
- Multiple PCBs connected with cables and/or backplanes
- Functionality defines the system, the PCBs & the required sub-system interconnect



## Platform-centric Systems

Mentor Solution:  
Capital Platform

- Interconnect defines the system
- Complete aerospace or automotive projects



# DxSystems Designer Overview

EE 7.9.5

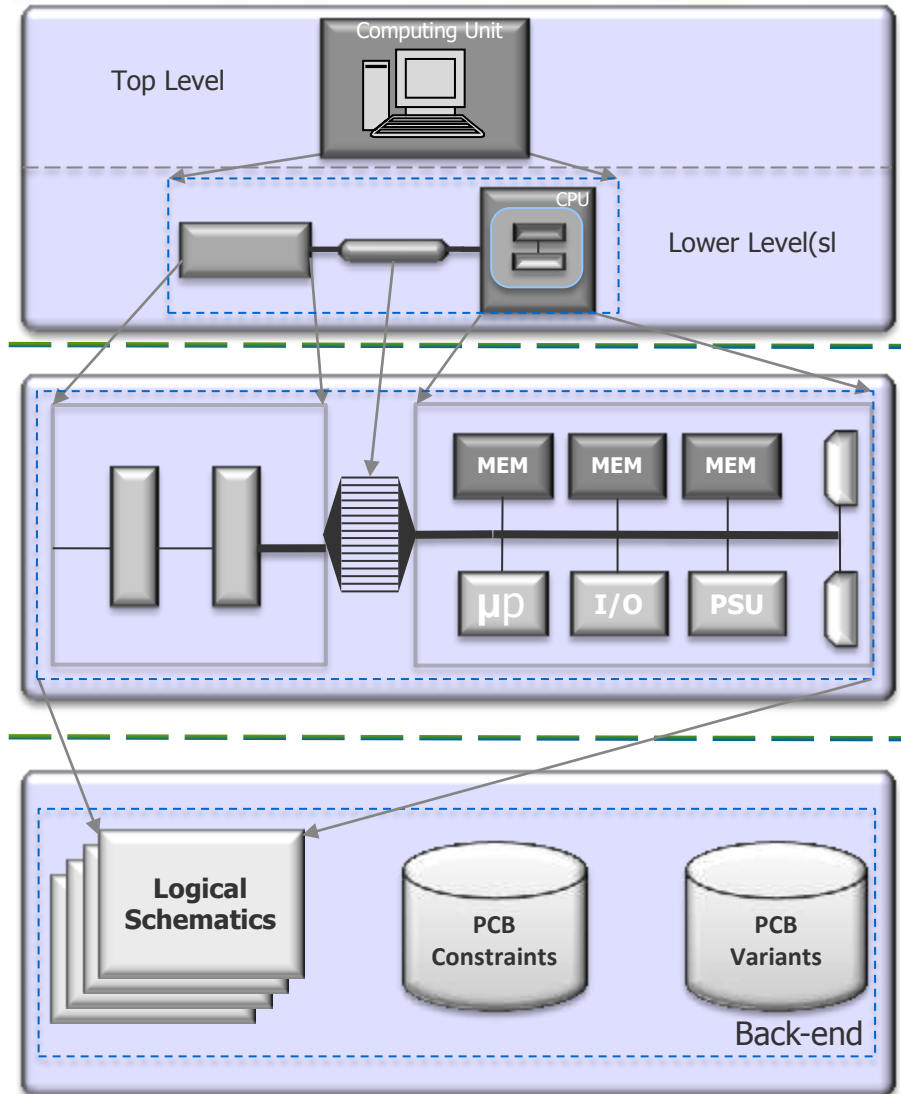
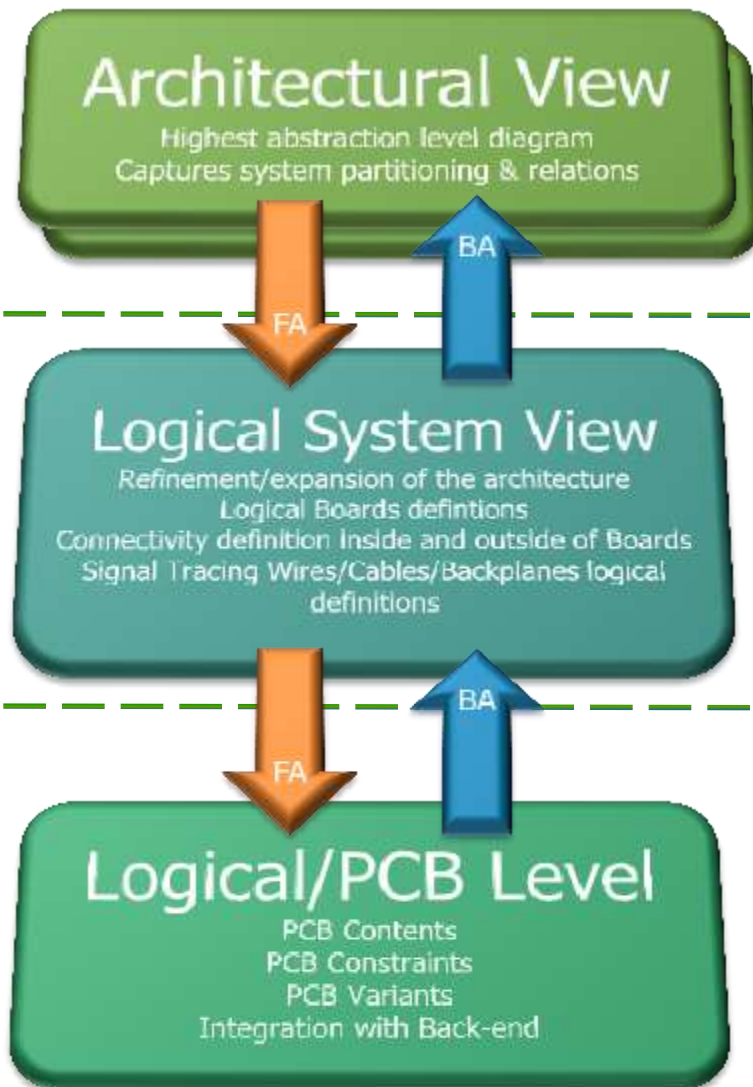
- DxSystems Designer captures the **hardware description of the system**
  - Starting from the architectural level through the logical system level down to the logical/PCB level including the logical definition of:
    - Wires, cables and backplanes
  - DxSystems Designer is targeted at the hardware implementation space
  - DxSystems Designer is not a functional simulation or a hardware/software co-verification development environment





# DxSystems Designer Structure Overview

EE 7.9.5



# Product Plans

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- DxDesigner
- DxSystems Designer
- Expedition, CES
  - Expedition / Xtreme 7.9.4 focus
  - CES
  - NPI
- DMS
- FPGA Design

# Release Themes

- Expedition / Xtreme PCB 7.9.4 focus:
  - Intelligently communicating design intent
    - From engineering to layout
    - From PCB design to manufacturing
  - Improving productivity
    - HDI routing
    - RF design

## Intelligently Communicating Design Intent

- Layout actuals process improvements
  - Simpler process reduces user errors
  - New format & mechanism used throughout flow
  - Settings to allow automatic update and export of actuals
  - Progress dialog added to front-end for Import Actuals
- Improved match group violations
  - Reduces possibility of user error when using hierarchical match groups
  - Automatic update of parent delay types when children are changed
- CES diagnostics run from Expedition can fix more errors

Constraint Class/Net	Length or TOF Delay			
	Type	Match	Tol (th)(ns)	Delta (th)
⊕ XINT_N5	Length			
⊕ XINT_N6^^^^	Length			
⊕ XINT_N7	Length			
⊕ Clocks	Length			
⊖ MatchedControl	Length		150	
⊕ CTRL_BITS0	Length			
⊕ CTRL_BITS1	Length			
⊕ CTRL_BITS2	Length			
⊕ CTRL_BITS3	TOF			
⊕ CTRL_BITS4	Length			
⊕ CTRL_BITS5	Length			
⊕ CTRL_BITS6	Length			
⊕ CTRL_BITS7	Length			
⊕ Busclass	Length			

# Manufacturing – Export ODB++ Intelligently Communicating Design Intent

EE 7.9.4

## ■ More intelligent ODB++

- Correct generated silkscreen layer naming
- Mounting hole tolerances
- Board embedded contours output when ODB++ generated from panels
- Mounting hole net connectivity
- User layer identified as ODB++ layer type document

## ■ Streamlined ODB++ generation

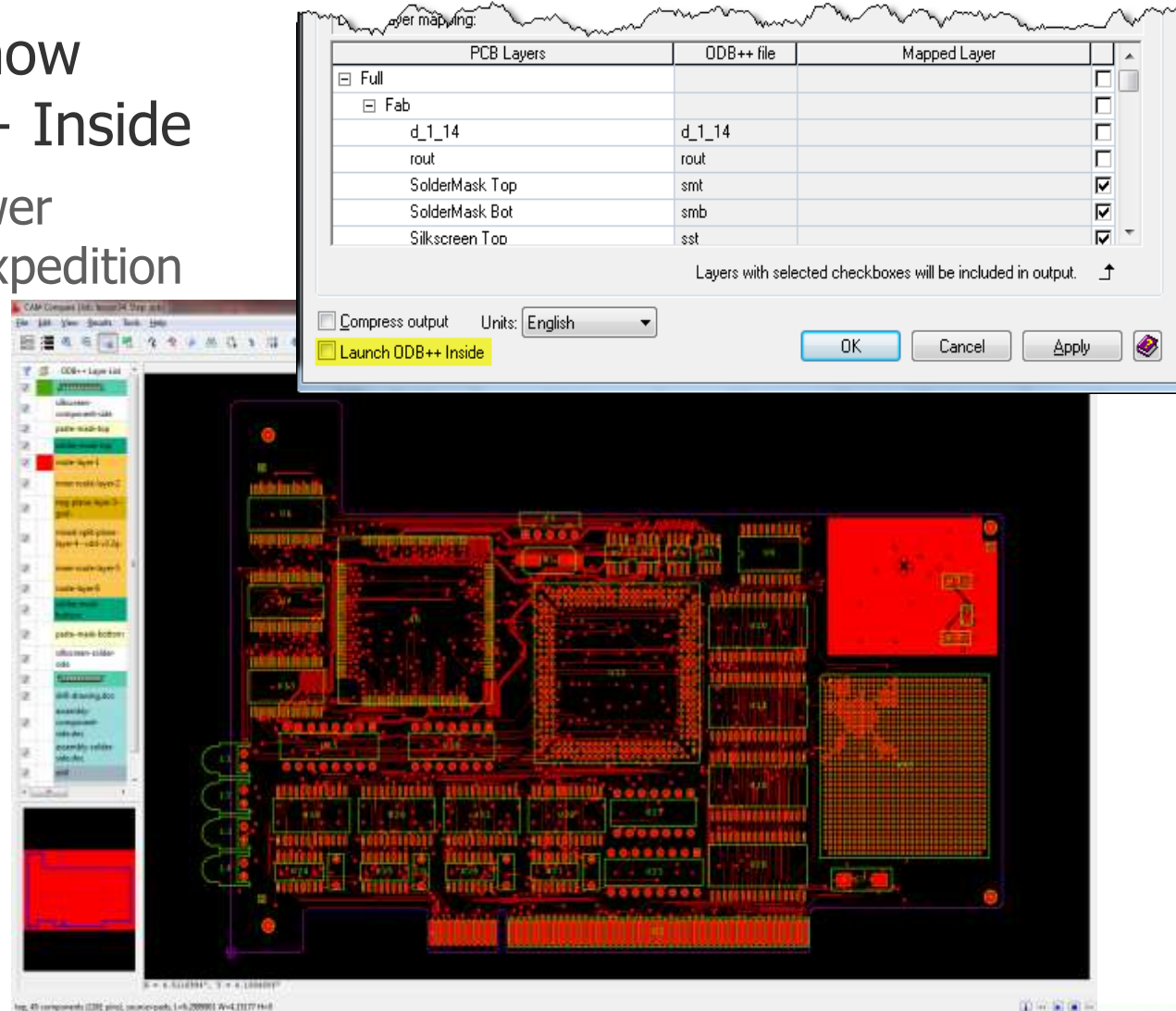
- Defaults for user layers

# Manufacturing – ODB++ Inside

## Intelligently Communicating Design Intent

EE 7.9.4

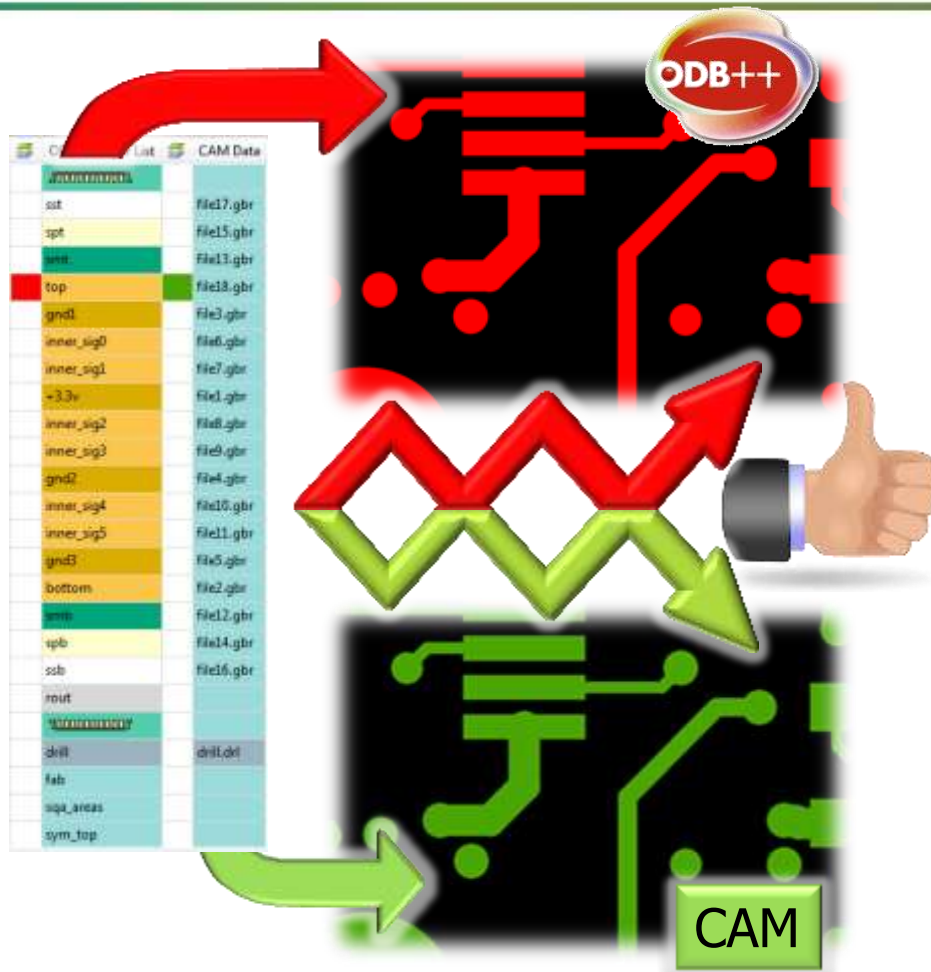
- Export ODB++ now launches ODB++ Inside
  - An ODB++ viewer included with Expedition PCB



# Manufacturing – CAM Compare

## Intelligently Communicating Design Intent

EE 7.9.4



- Compares ODB++ to traditional CAM
  - Gerber 274X – Design Data
  - Excellon – Drill Data
- Confirms EDA netlists for correctness
  - Both ODB++ and IPC-D-356A
- Enables a smooth transition to ODB++
  - Reduce time-to-market
  - Minimize the NPI cycle
- Maintain design integrity
  - Improve quality by preventing errors before they happen
- Streamline communication
  - Seamless integration between design and manufacture
- Reduce data storage requirements
  - Integrated data with no redundancy

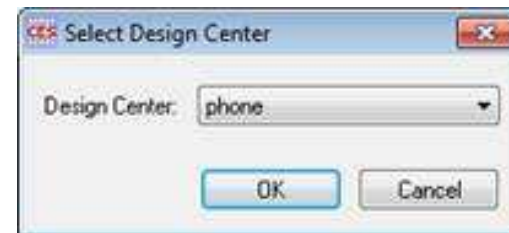
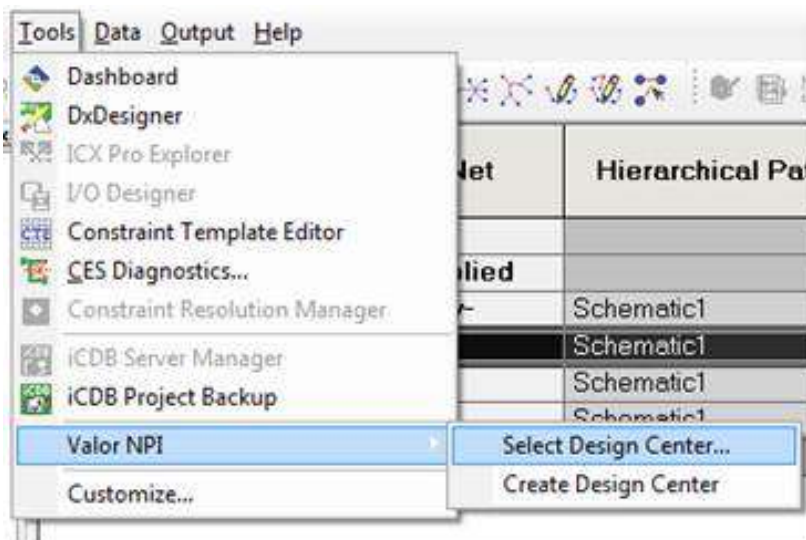
**Now included with Expedition PCB**

# Valor NPI Design Center in CES

## Intelligently Communicating Design Intent

EE 7.9.4

- Valor NPI Design Center defines reusable setup
- Select or create Design Center in CES
- Persistence of Design Center across Valor NPI runs





# Expedition PCB

## Improving Productivity

EE 7.9.4

- Easier manipulation of HDI via stacks with Dynamove
  - Move as a complete stack
  - Move individual vias from within the stack
  - Single or multi-via stacks
  - Supported in Expedition PCB & Xtreme PCB

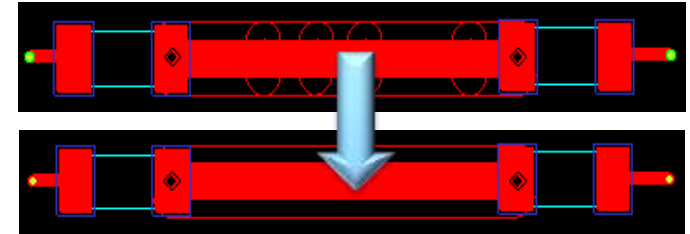
# RF Meander Enhancements

## Improving Productivity

EE 7.9.4

### ■ Enhanced RF meander routing

- Fast creation of 2 point meanders
  - Odd angle and off grid connections
- Meander plane clearance simplified
  - Co-linear meander segments combined
- Smart editing of meanders
  - Maintaining bend angles and miters during segment move
  - Snapping meander ends to component pins
  - User controlled removal of bends
- Meander “effective length” control



# Product Plans

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- DxDesigner
- DxSystems Designer
- Expedition, CES
- DMS
  - 7.9.4 Content Summary
  - Simulation Model Integration
  - 3<sup>rd</sup> Party Integration (EDX)
  - EDX Based DMS Library Cache Update
  - Library Process Improvement
- FPGA Design

# DMS 7.9.4 Planned Content

## Usability Enhancements

- Viewable part hierarchy updates upon part release
- Partition sorting for easier component mapping
- Continued load after single part failure

## Variant Manager Interface Enhancements

- Integration improvements with Variant Manager
- Part replacement for Variants from DMS (BETA)

## Performance/Cache Updates

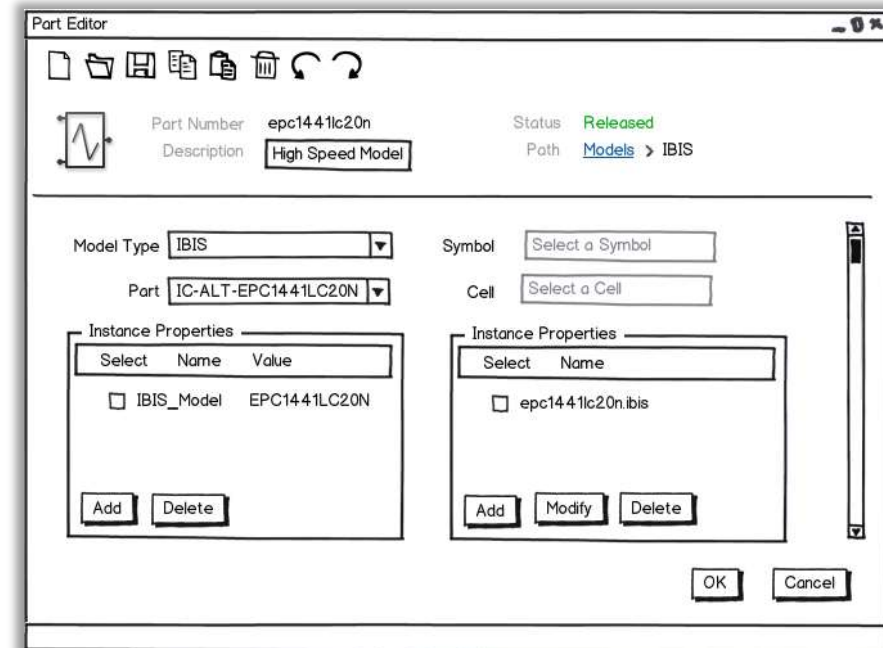
- Adding support to Modify Pins for symbols with more than one mapping
- Adding support to Modify Pins to recognize specific symbol versions

## Reuse Block Management

- Checks to limit simultaneous edits on reuse block

# Simulation Model Integration

- Provide an ITK (Integration Tool Kit) to support the addition of simulation models to the library
  - Model to Part registration allowing for the addition of simulation models without impacting the PCB library
  - Model editor registration
  - Out of the box support for the HyperLynx analysis models
- Adds value to the existing PCB library
  - Simulation experts can add models without impacting the existing library data
  - Users can “like” models to indicate approval



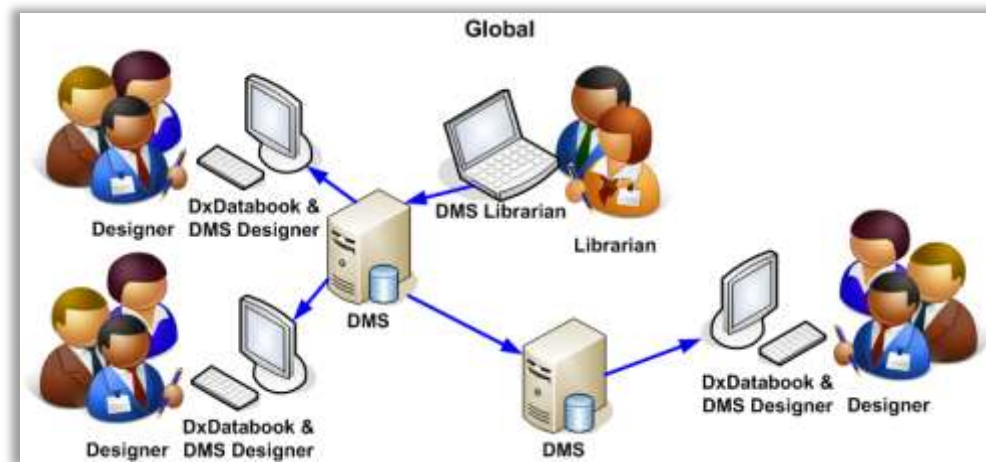
# 3<sup>rd</sup> Party Integration (EDX)

- EDX is Mentor's Enterprise Data Exchange Format
  - Version-independent data format for design and library data
  - Single file to systematically exchange between Expedition Enterprise and 3<sup>rd</sup> party systems
- EDX generation of:
  - Component/Supplier Data
  - WIP Partlist (BOM) Integration
  - Part Request Integration
  - Library Distribution
- Promotes more direct, consistent integration with 3<sup>rd</sup> parties



# Library Process Improvements

- Improved integration with EE Editors
- Automatic part creation
- Simplified library environment
- Improved library verification
- Added support for library version management



# Product Plans

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- DxDesigner
- DxSystems Designer
- Expedition, CES
- DMS
- **FPGA Design**
  - I/O Designer
  - Precision



# I/O Designer: EE 7.9.4

## ■ New FPGA Vendors Device Libraries & S/W Support

- Xilinx ISE 13.4
  - Zync devices - new
  - Artix 7I devices - new
- Actel Designer 9.1 SP4
- Altera Quartus 11.1 SP2
  - Arria V devices - new

## ■ Newly integrated HDL parsers: VHDL, Verilog

- Matching MGC FPGA design solutions (e.g. Precision)

## ■ Unraveling enhancements

## ■ Symbol generation enhancements

## ■ Internal VREF support



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